

FIG. 1

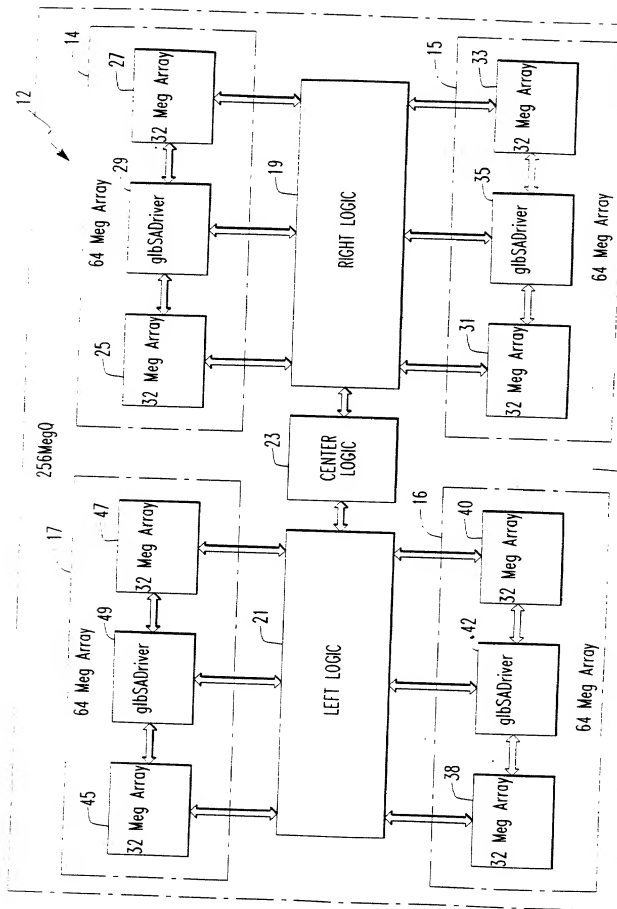
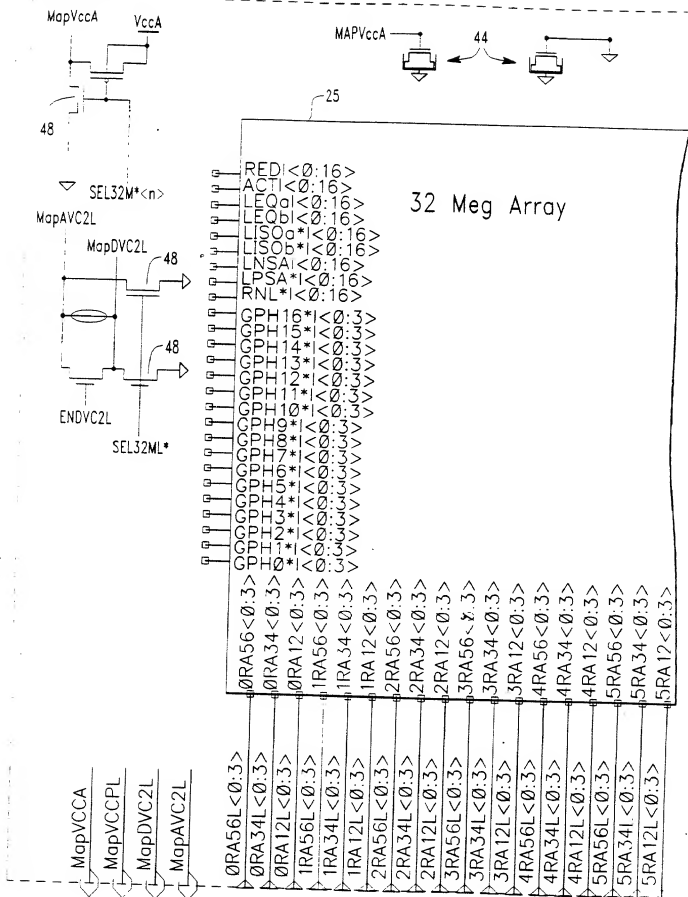


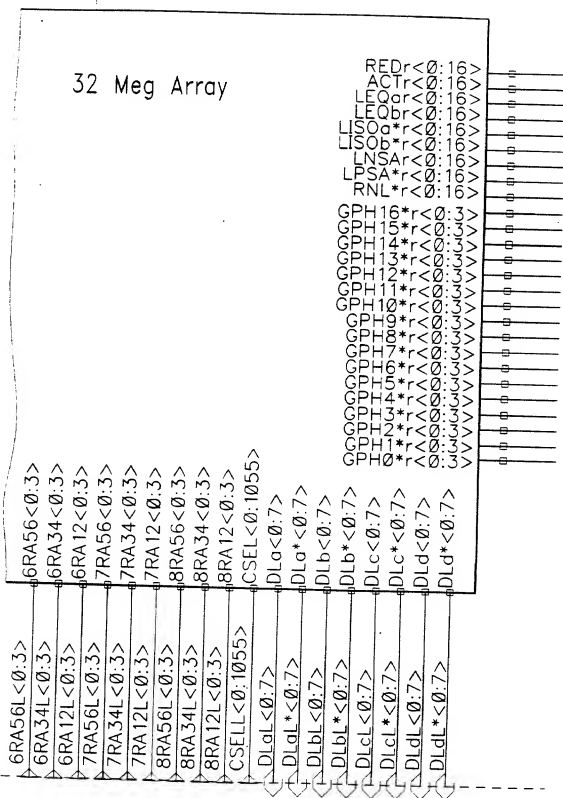
FIG. 2

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**Figure 6**



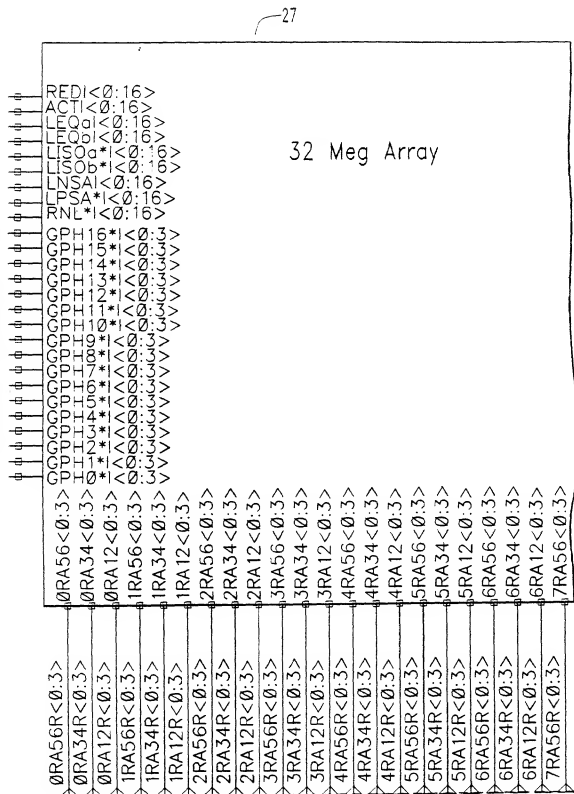
1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000 13000 14000 15000 16000 17000 18000 19000 20000 21000 22000 23000 24000 25000 26000 27000 28000 29000 30000 31000 32000 33000 34000 35000 36000 37000 38000 39000 40000 41000 42000 43000 44000 45000 46000 47000 48000 49000 50000 51000 52000 53000 54000 55000 56000 57000 58000 59000 60000 61000 62000 63000 64000 65000 66000 67000 68000 69000 70000 71000 72000 73000 74000 75000 76000 77000 78000 79000 80000 81000 82000 83000 84000 85000 86000 87000 88000 89000 90000 91000 92000 93000 94000 95000 96000 97000 98000 99000 100000



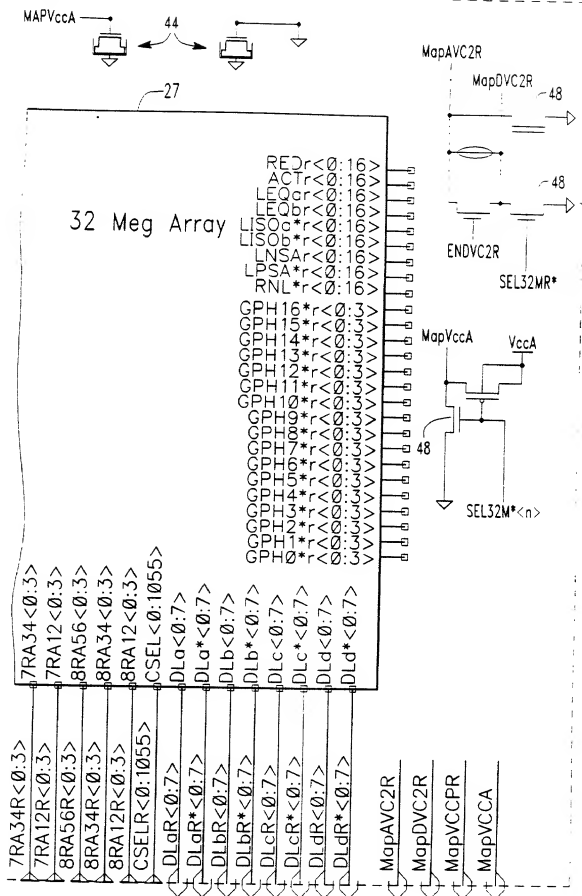


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[illegible]



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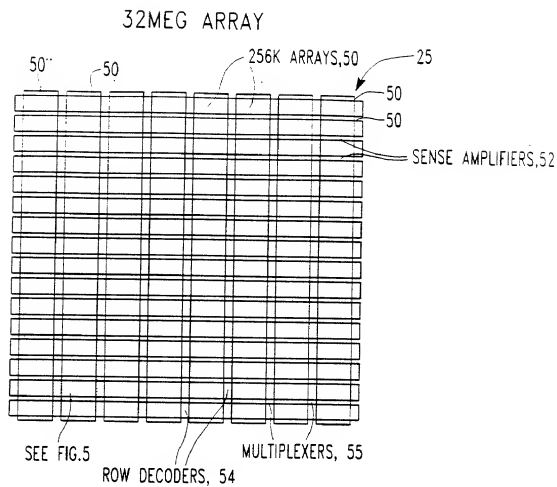


FIG. 4

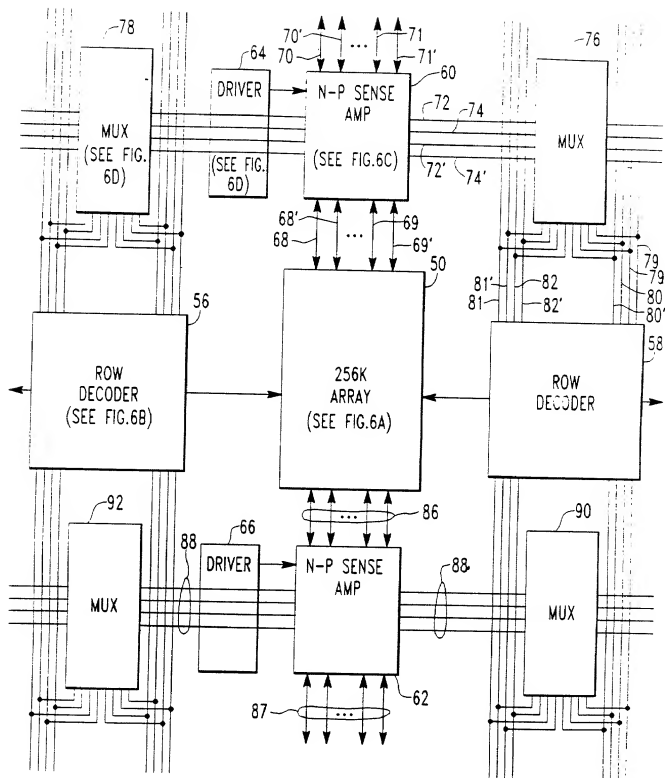


FIG. 5

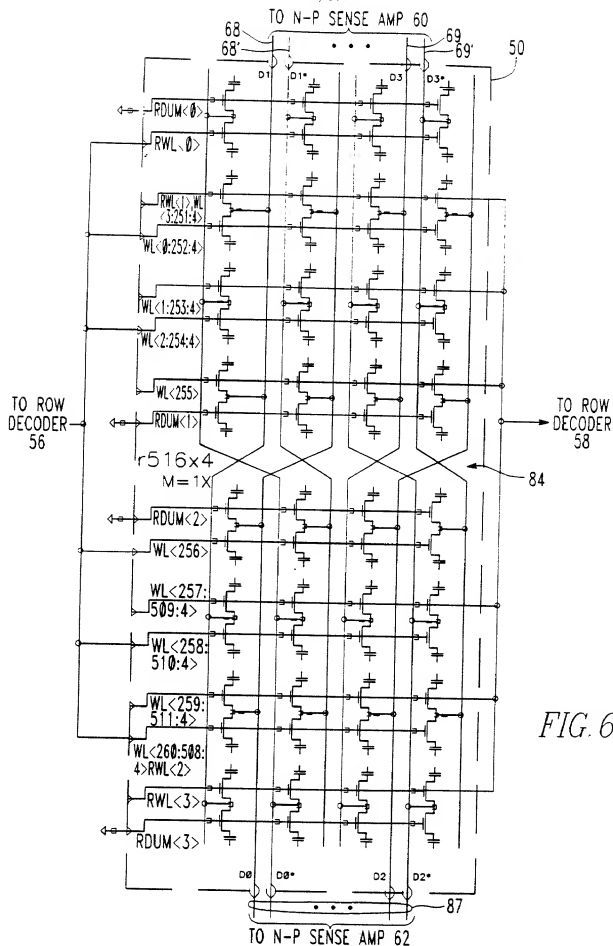
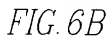


FIG. 6A



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Connections of odd/even  
columns to IOa and IOb  
alternates with odd/even  
column select lines:

CA01\* D1(even) D2(odd)

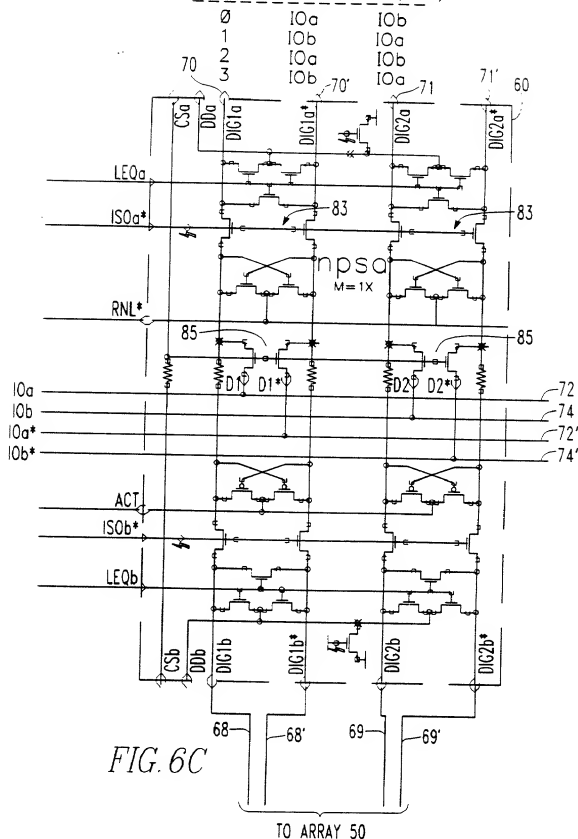


FIG. 6C



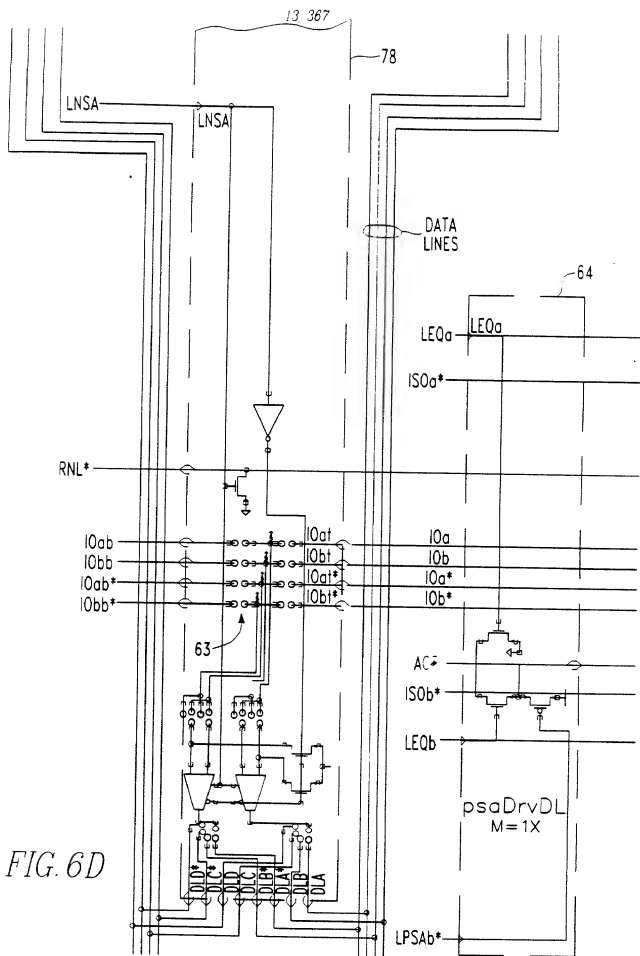


FIG. 6D

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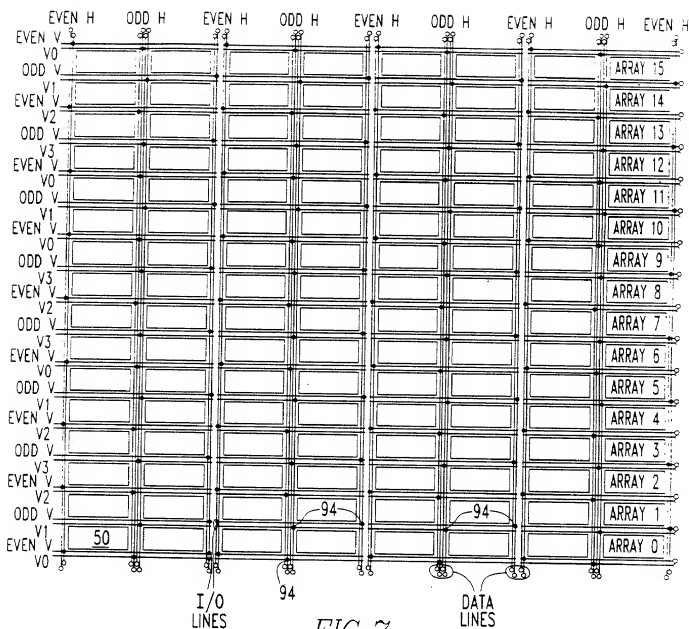
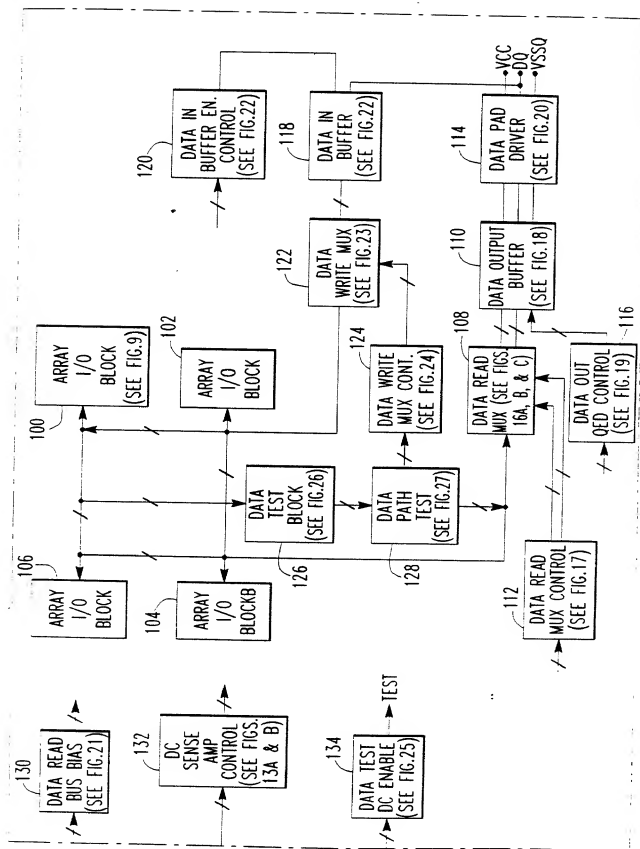


FIG. 7



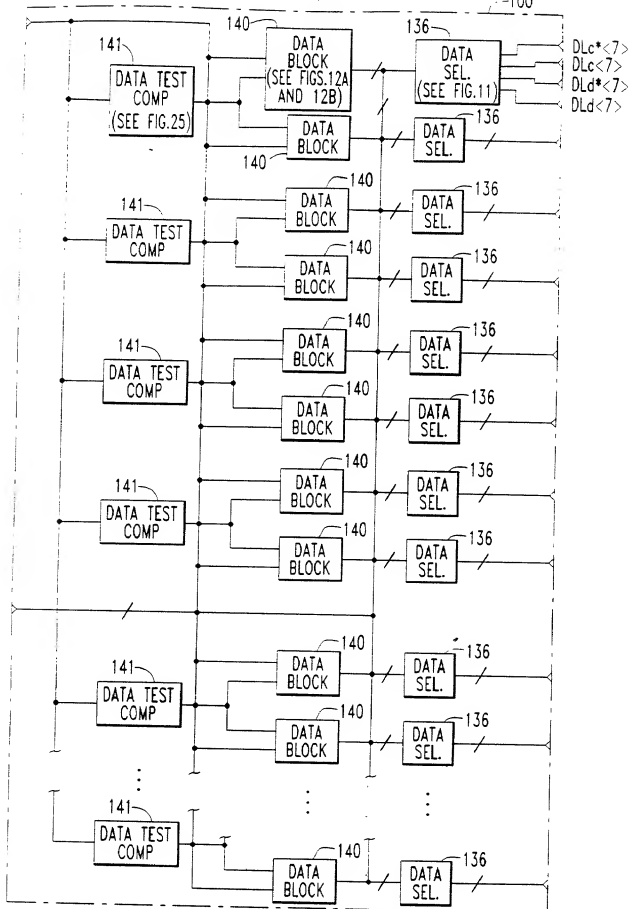


FIG. 9

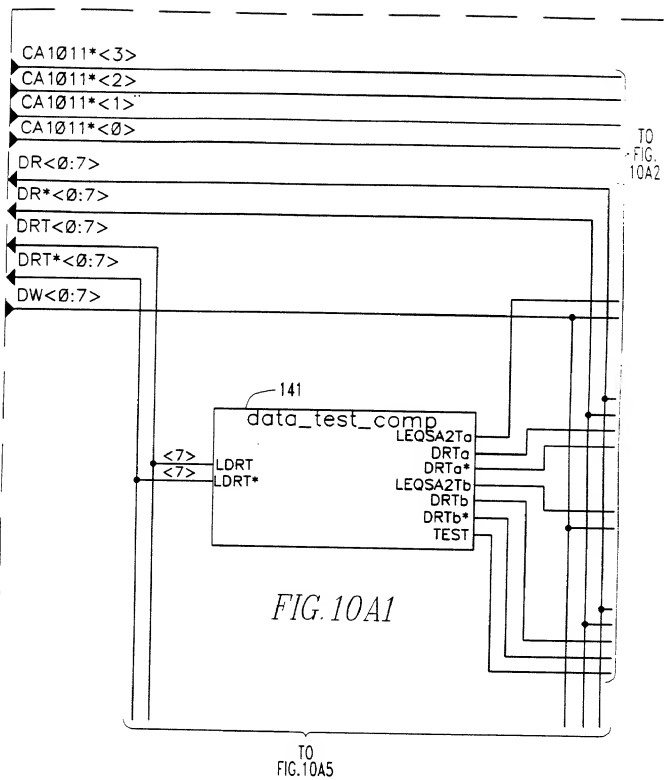


FIG. 10A2

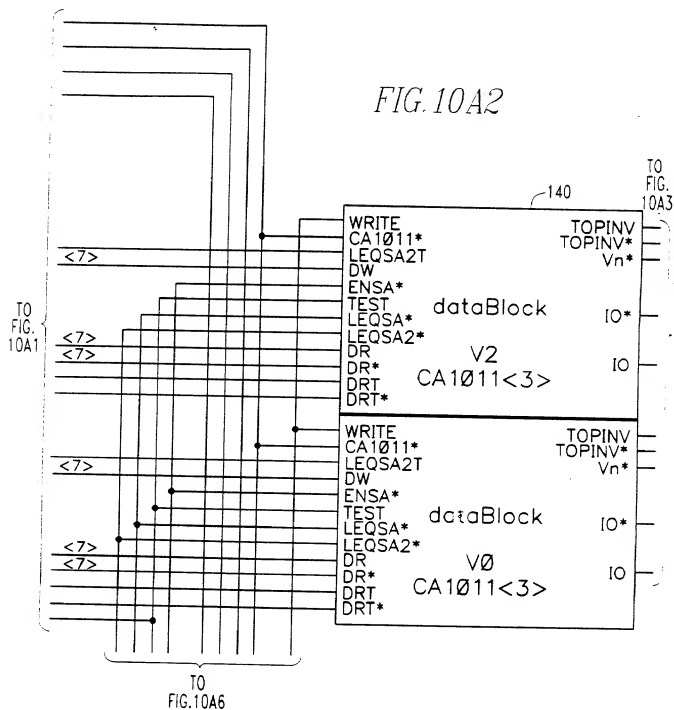
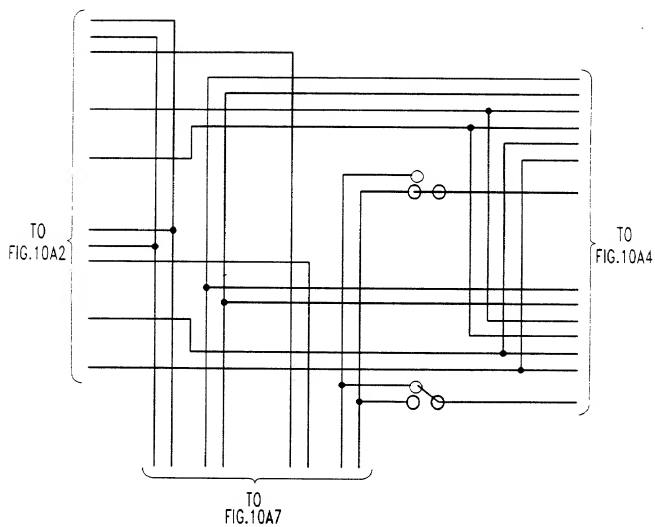


FIG. 10A3







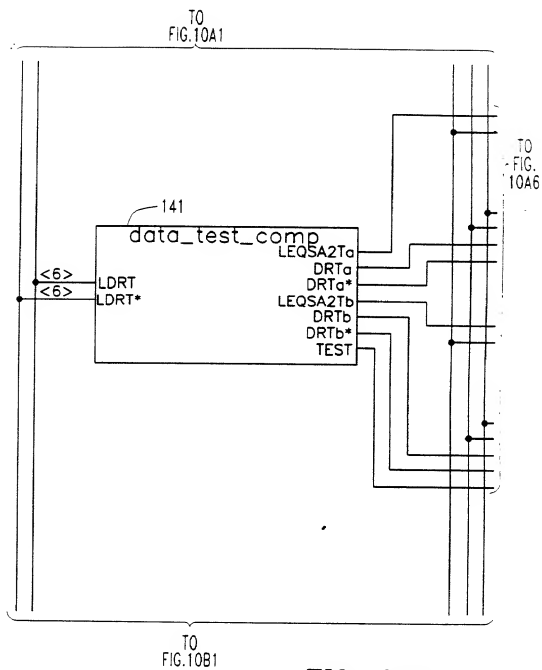


FIG. 10A5

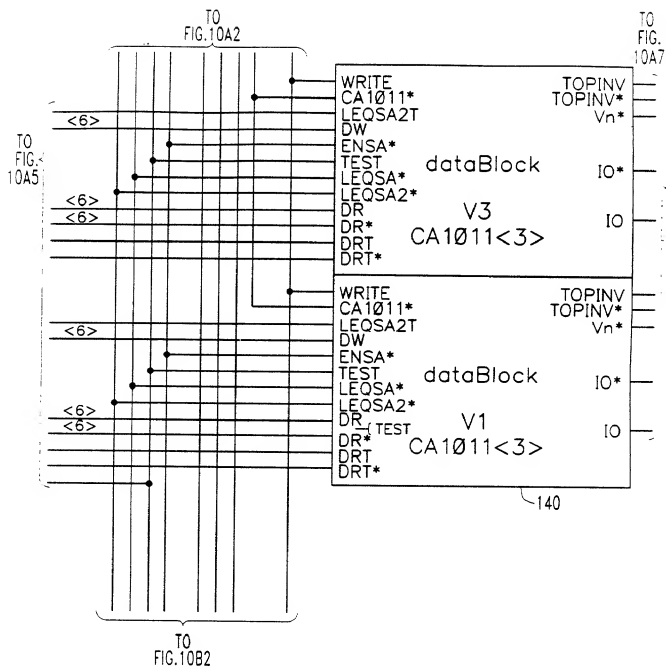


FIG. 10A6

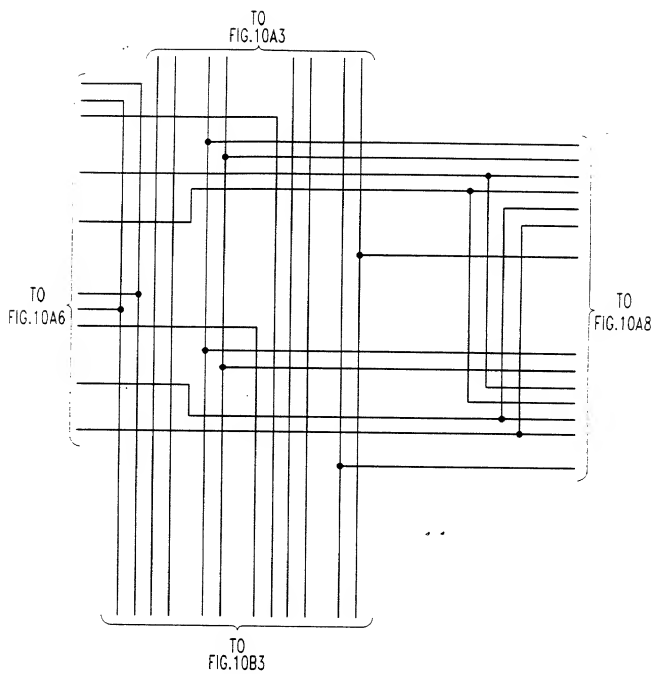


FIG. 10A7

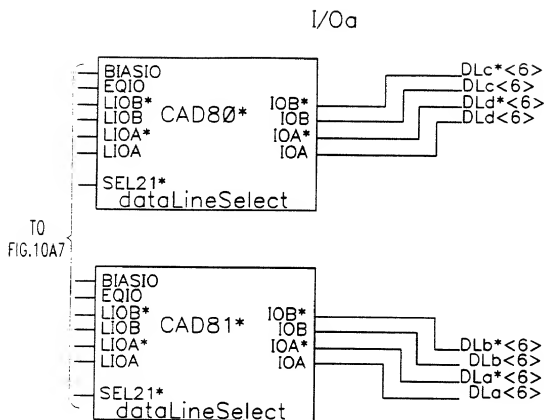


FIG. 10A8

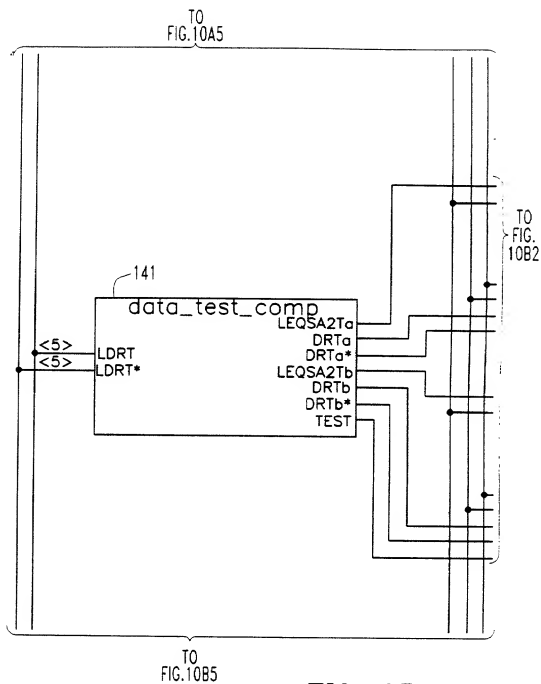


FIG. 10B1

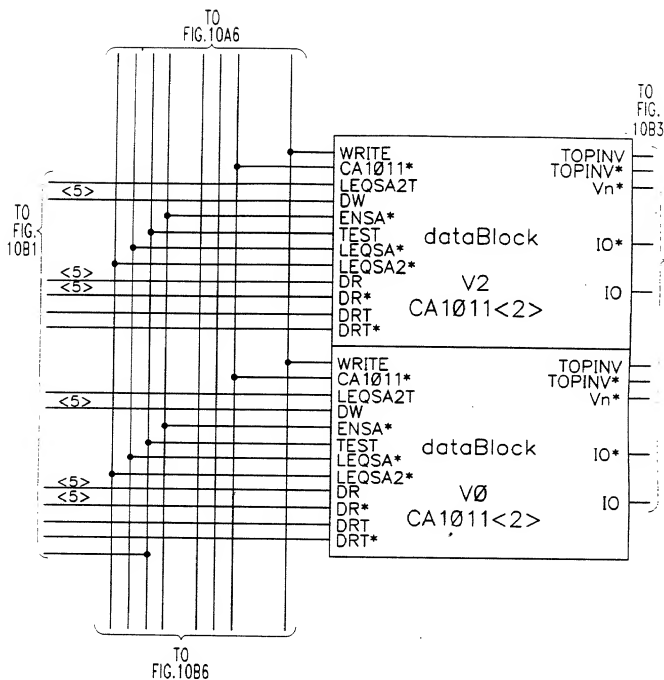


FIG. 10B2

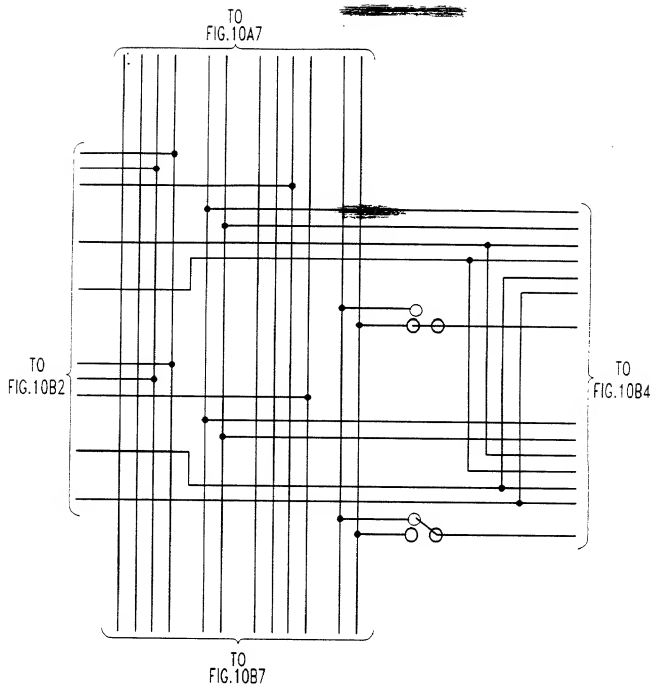


FIG. 10B3

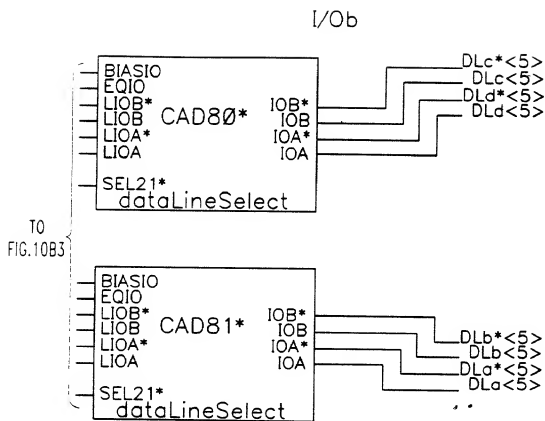


FIG. 10B4



FIG. 10B5

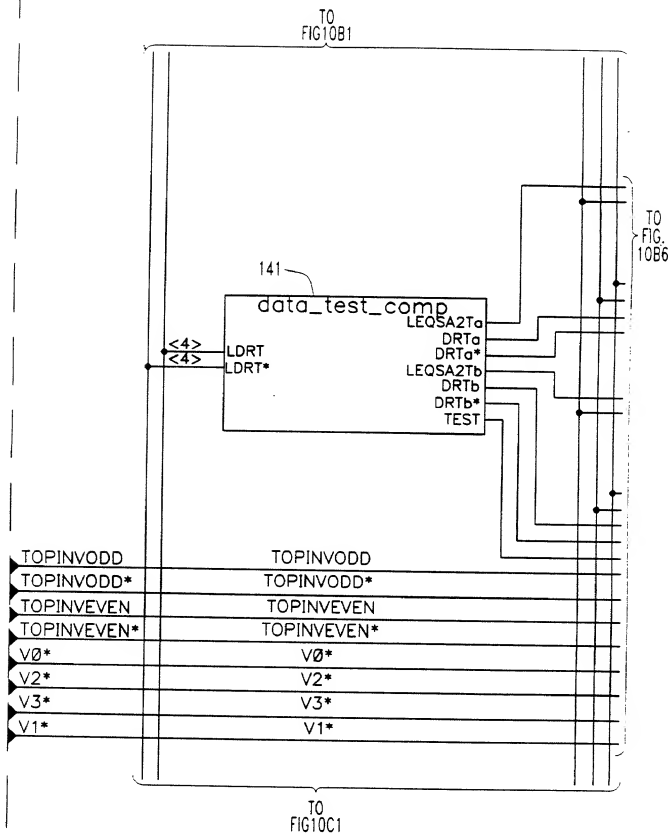


FIG. 10B6

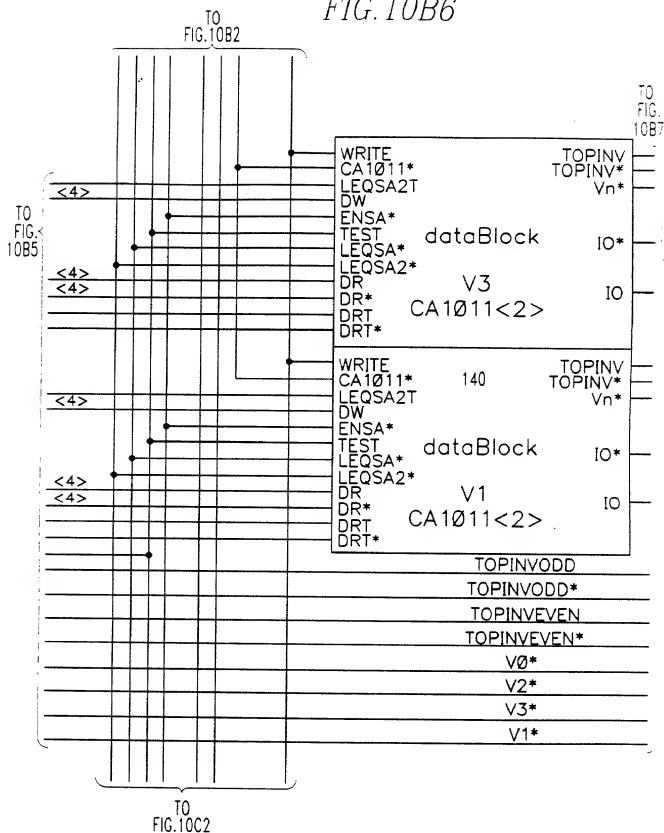


FIG. 10B7

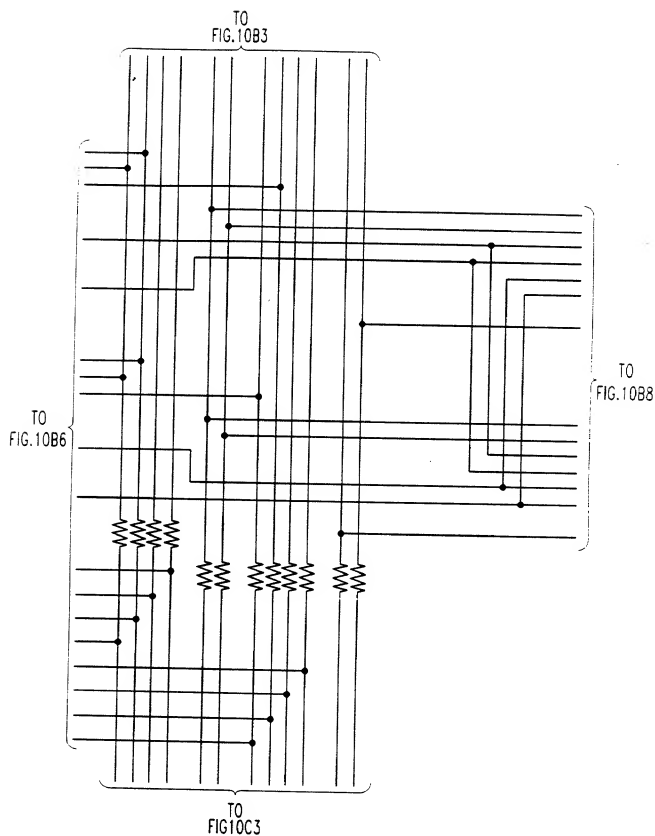
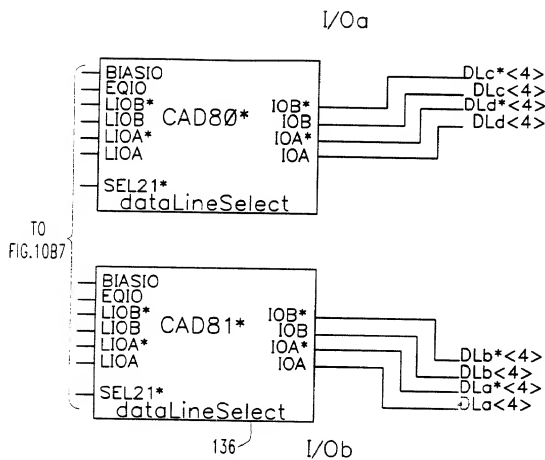
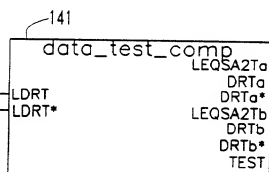
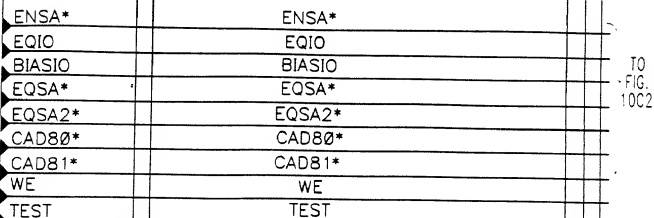


FIG. 10B8



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TO  
FIG. 10B5



TO  
FIG. 10C5

FIG. 10C1

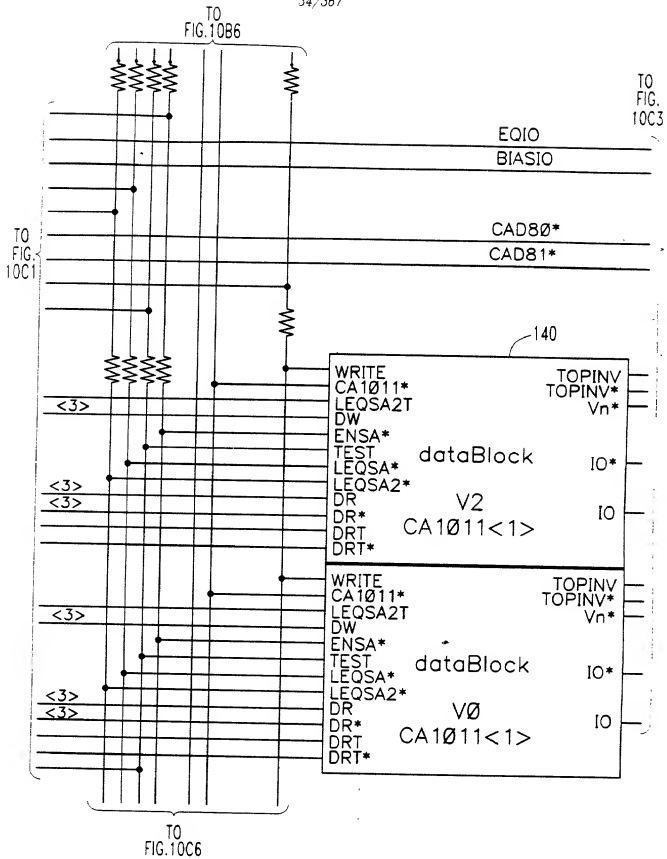


FIG. 10C2

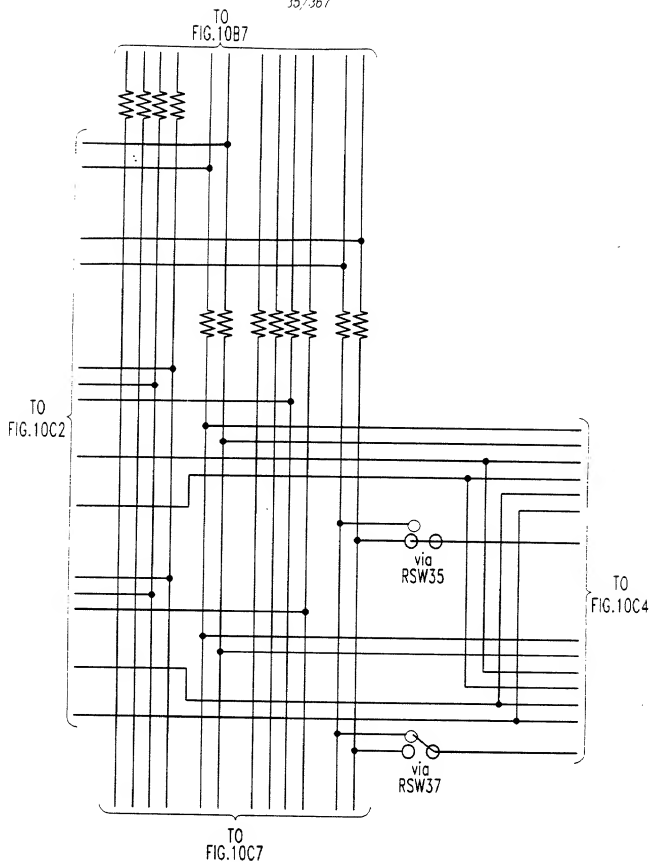
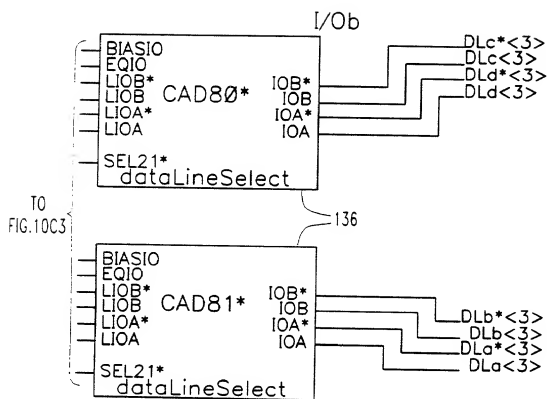


FIG. 10C3

FIG. 10C4





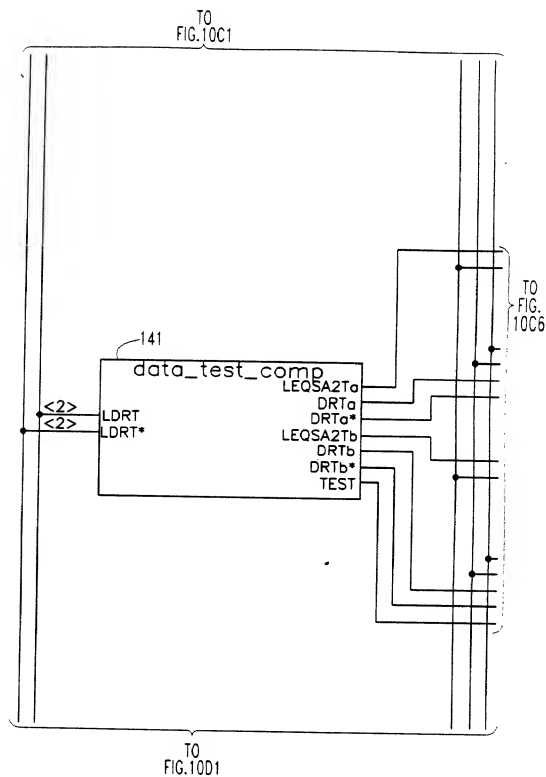


FIG. 10C5

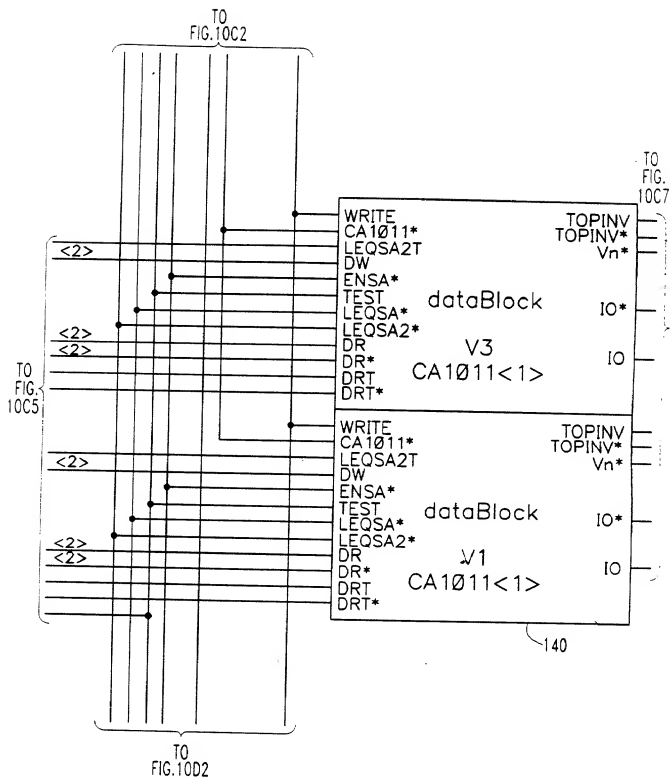


FIG. 10C6

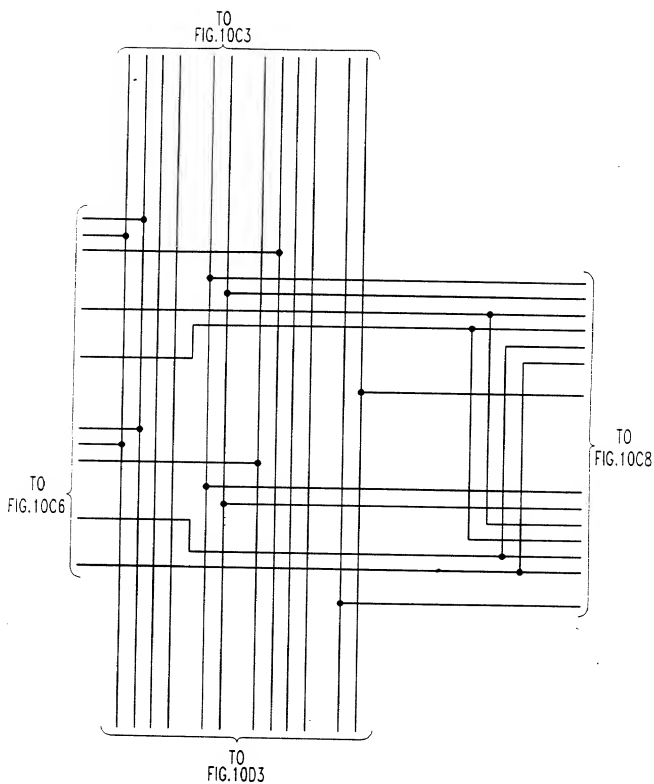


FIG. 10C7

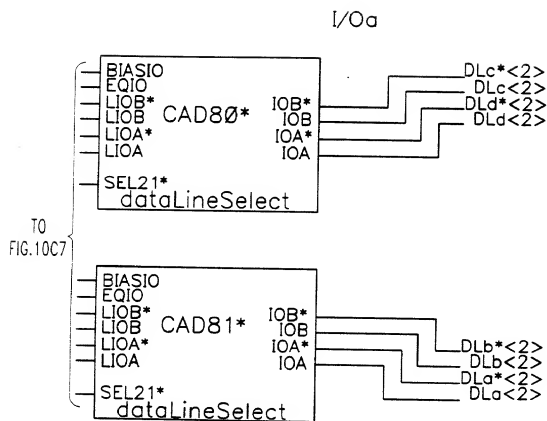


FIG.10C8

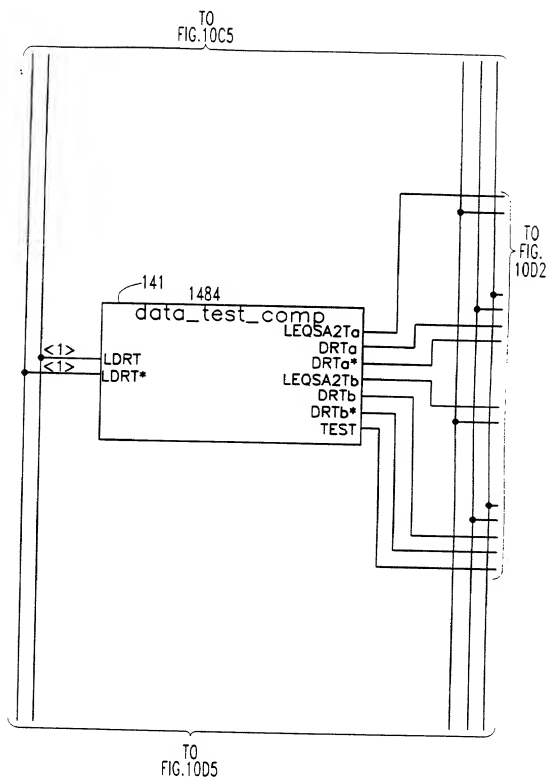


FIG.10D1

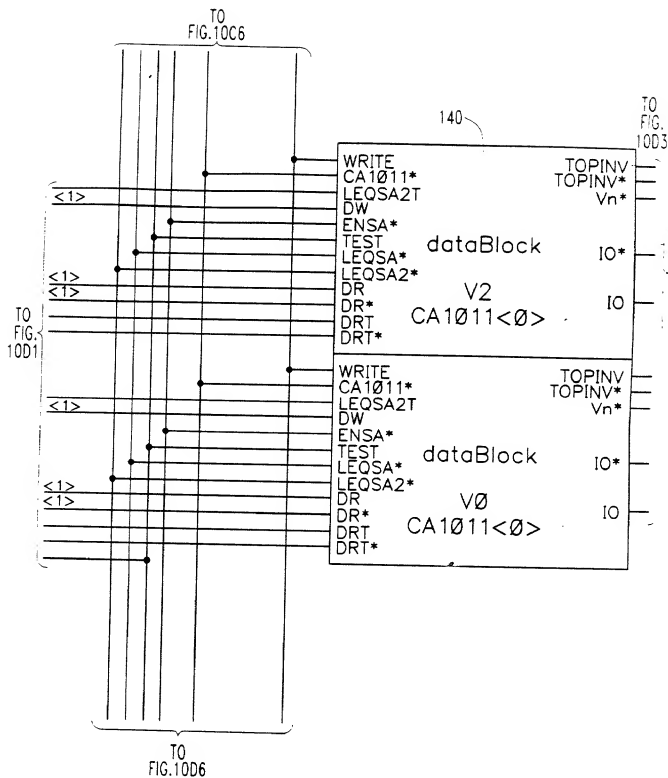
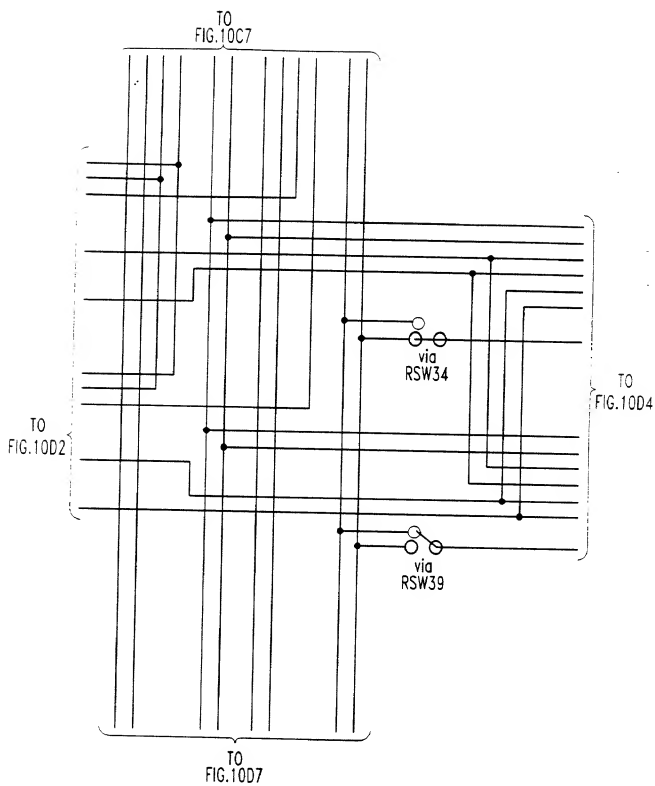


FIG. 10D2

*FIG. 10D3*

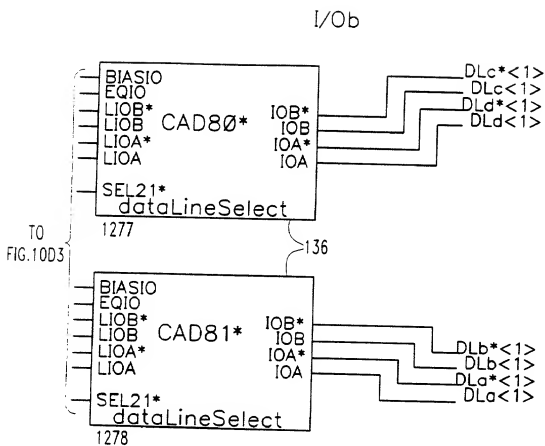


FIG. 10D4



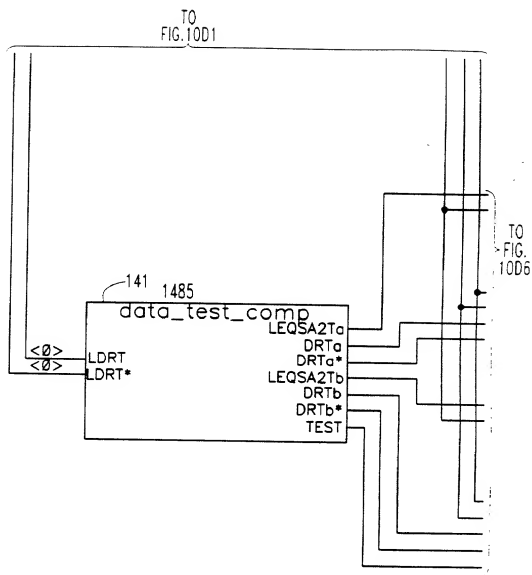


FIG. 10D5

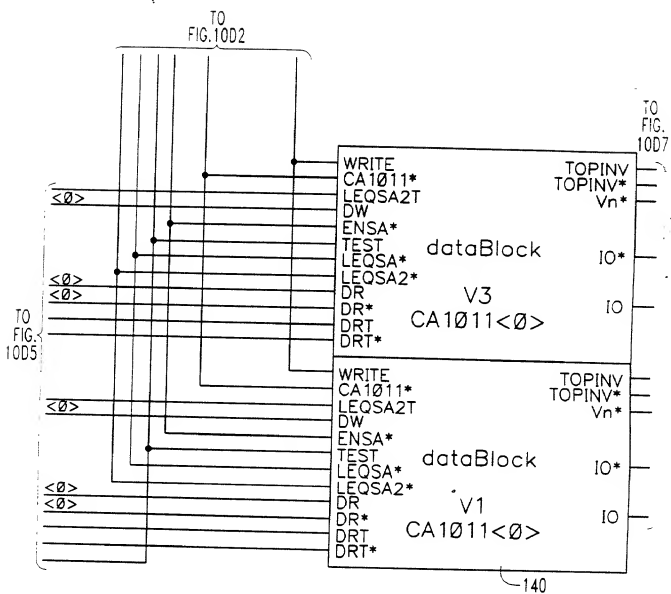
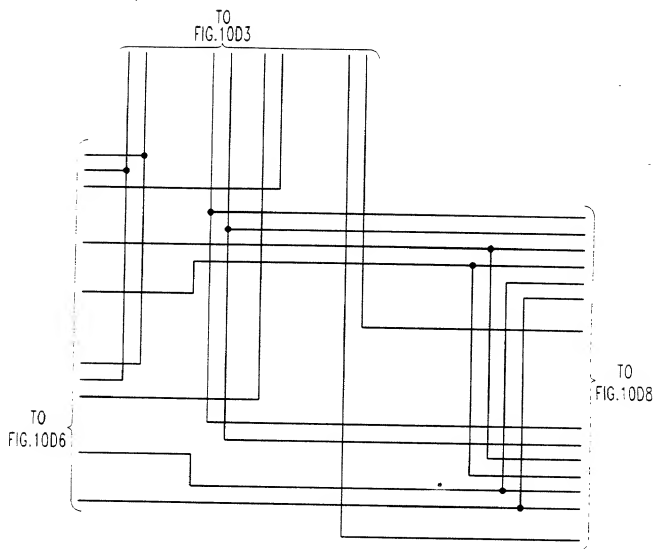


FIG. 10D6



---

*FIG. 10D7*

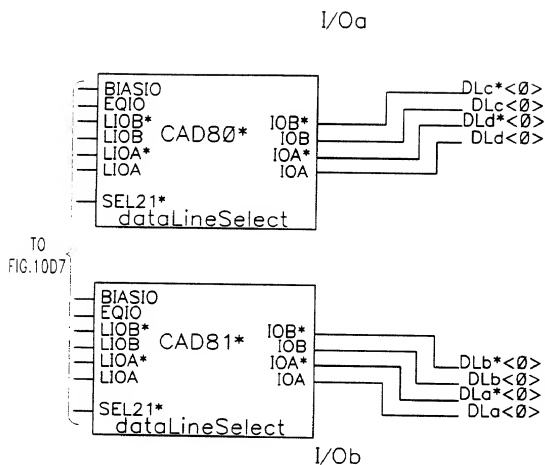


FIG. 10D8

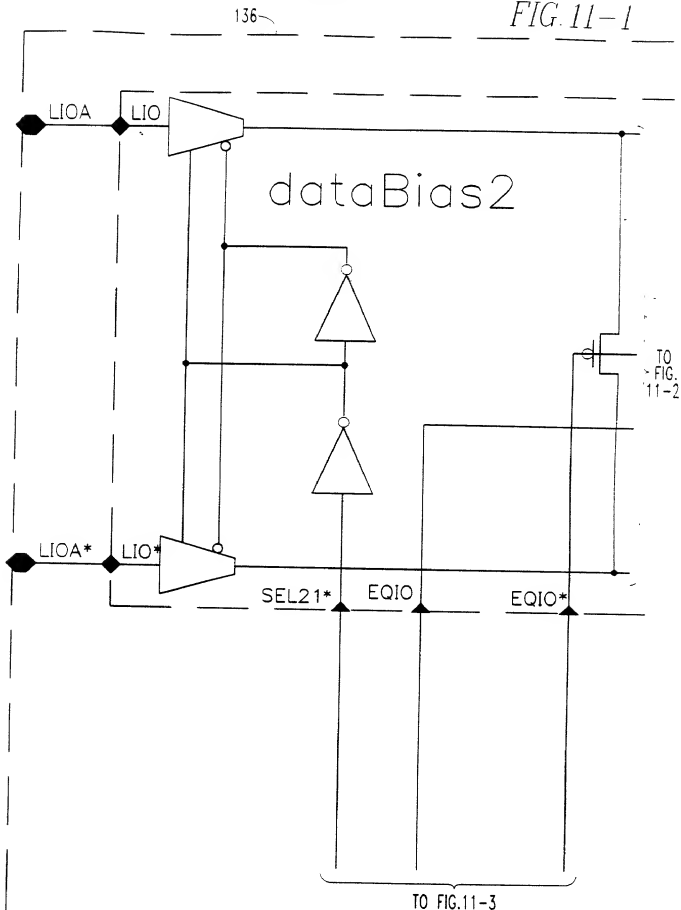
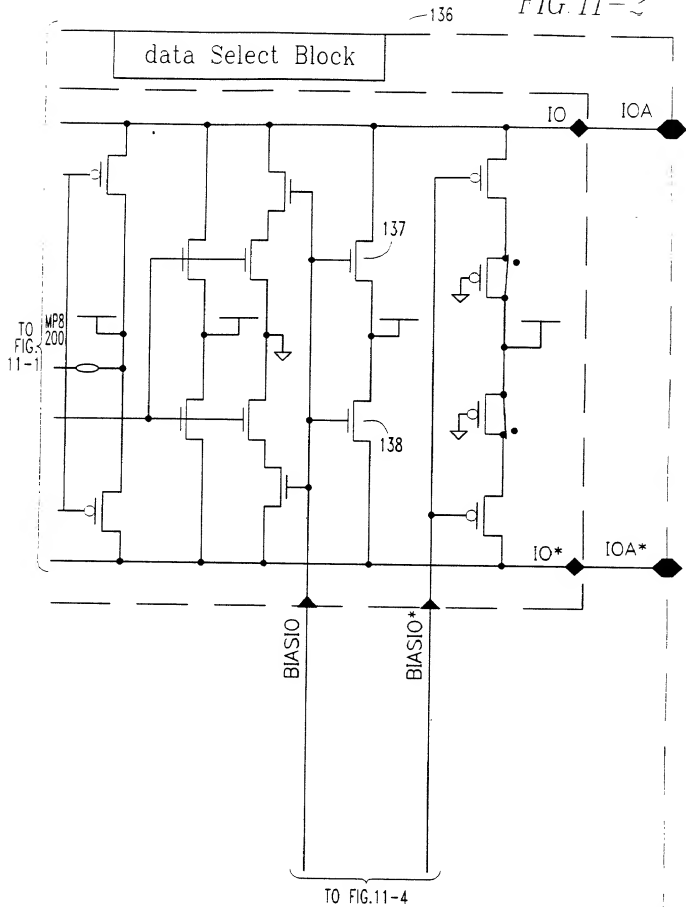


FIG. 11-2



51.367

TO FIG.11-1

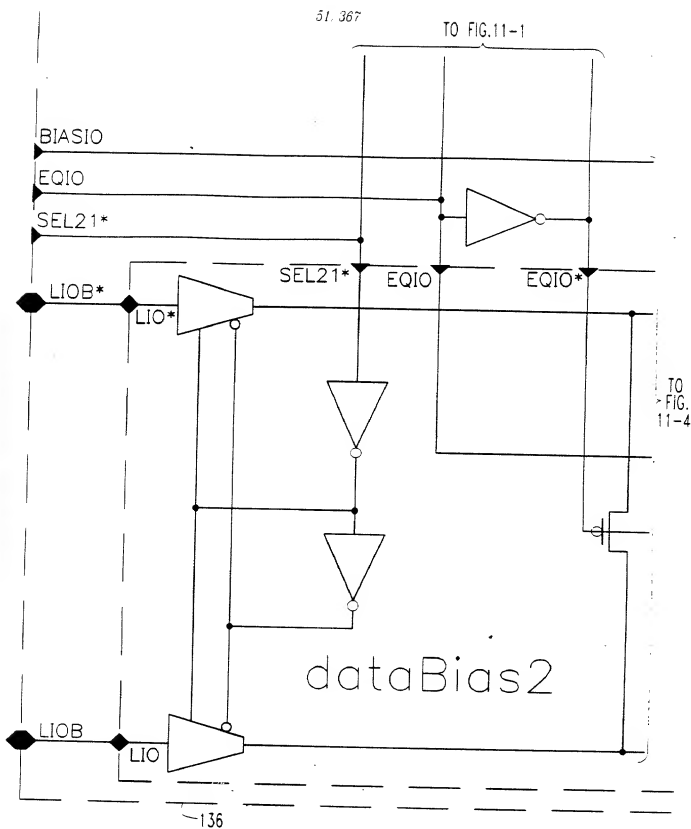


FIG. 11-3

TO FIG.11-2

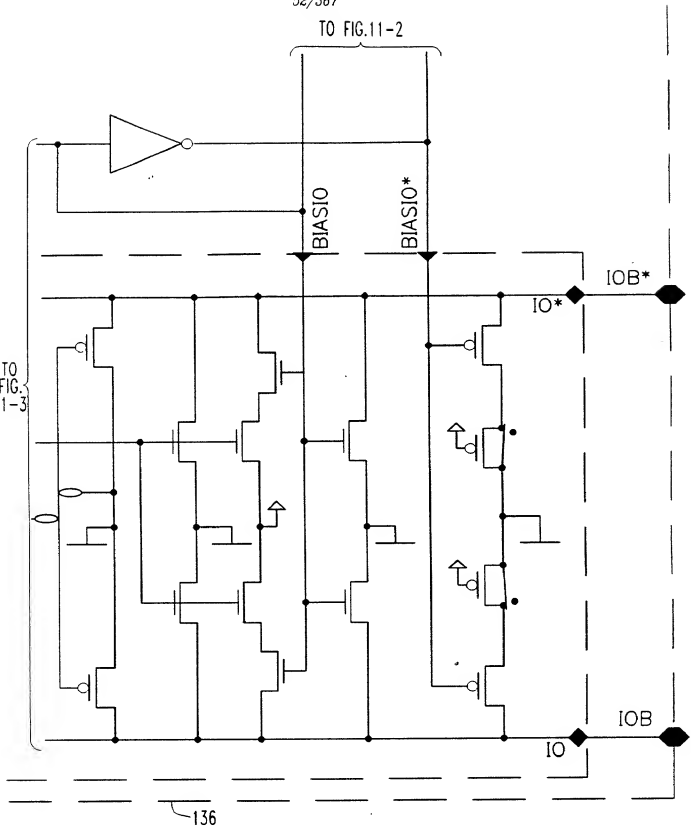
TO  
FIG.  
11-3

FIG.11-4





FIG. 12A2

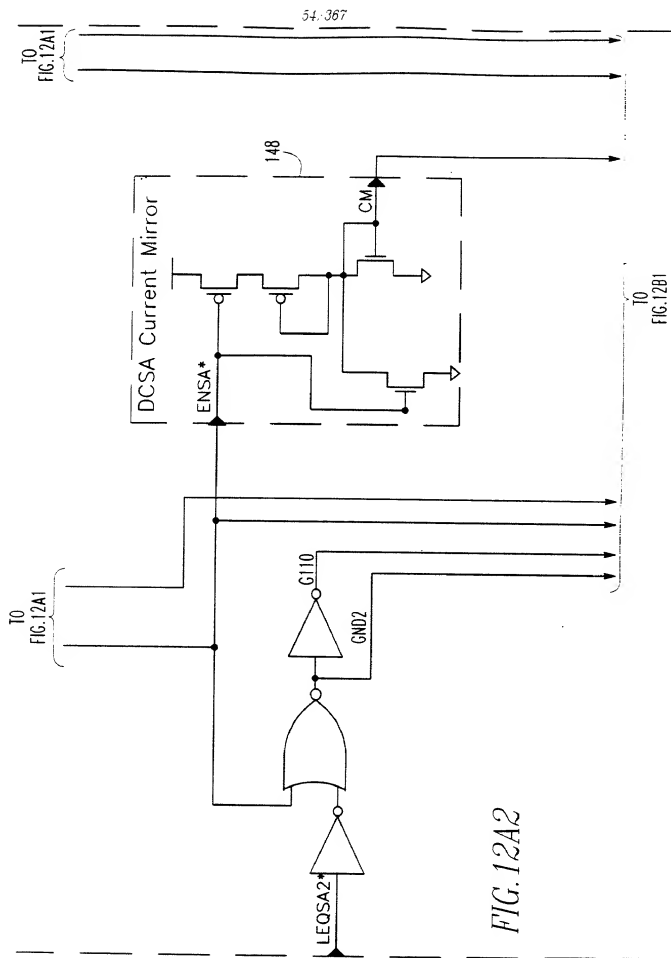


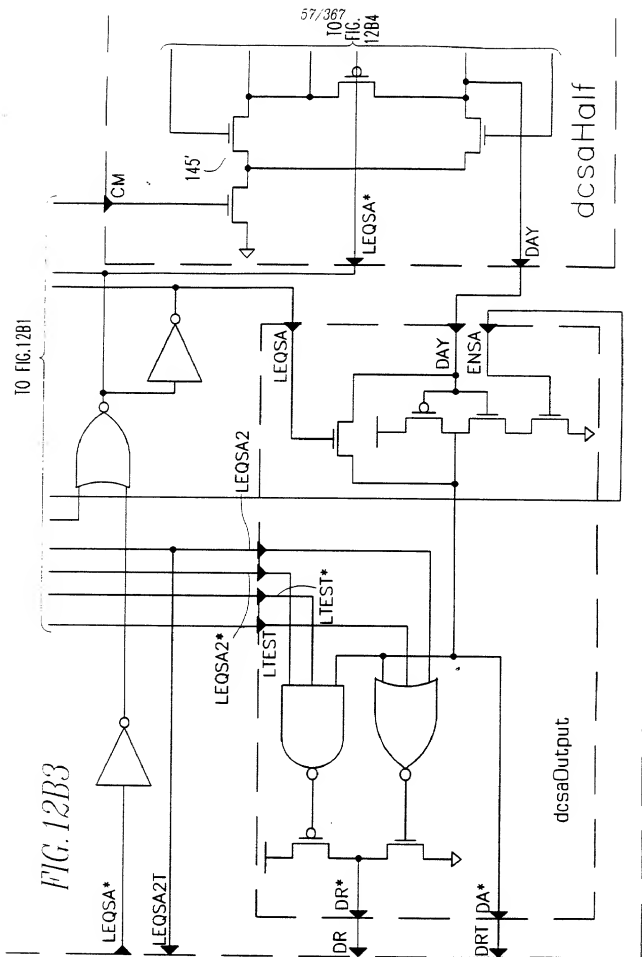
FIG. 12B1

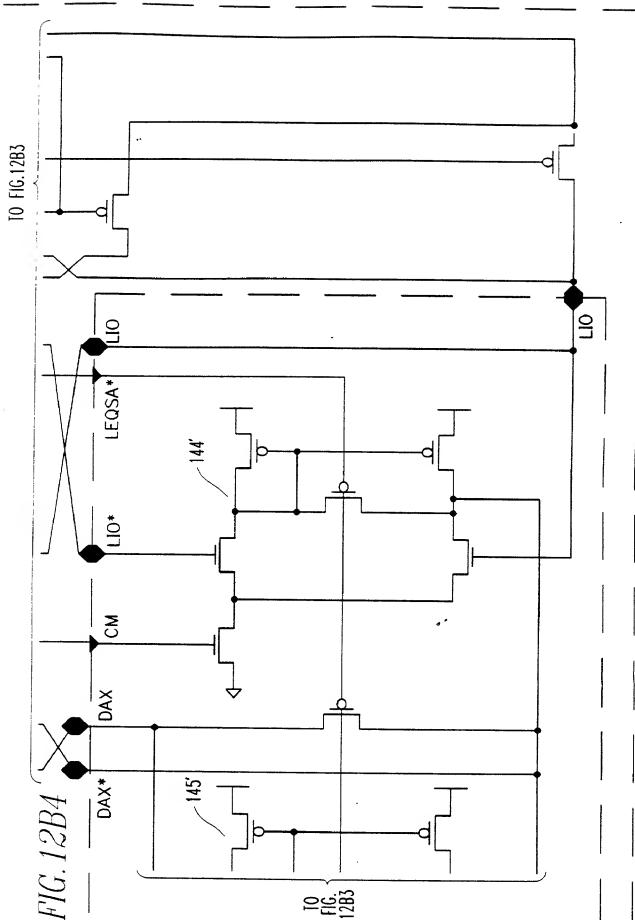
FIG. 12B1 is a circuit diagram showing a control logic block labeled **dcsaOutput** and a differential pair block labeled **dcsaHalf**. The **dcsaOutput** block contains an OR gate, an AND gate, and an inverter. The **dcsaHalf** block contains a differential pair of transistors with a current source 145. Various control signals are shown, including **DAY**, **LEQSA**, **ENSA**, **LEQSA2**, **LEQSA2\***, **LTEST**, **LTEST\***, **TEST**, **DRT\***, **DA\***, **DR\***, and **DR\***. The diagram also shows timing diagrams for **DRT\***, **DA\***, **DR\***, and **DR\*** at the bottom. The circuit is connected to a common mode signal **CM** and a test signal **TEST**. The output of the **dcsaOutput** block is connected to the **dcsaHalf** block. The **dcsaHalf** block is connected to a common mode signal **CM** and a test signal **TEST**. The circuit is also connected to a common mode signal **CM** and a test signal **TEST**. The output of the **dcsaOutput** block is connected to the **dcsaHalf** block. The **dcsaHalf** block is connected to a common mode signal **CM** and a test signal **TEST**. The circuit is also connected to a common mode signal **CM** and a test signal **TEST**.

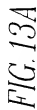
FIG. 12B3 TO



FIG. 12B3







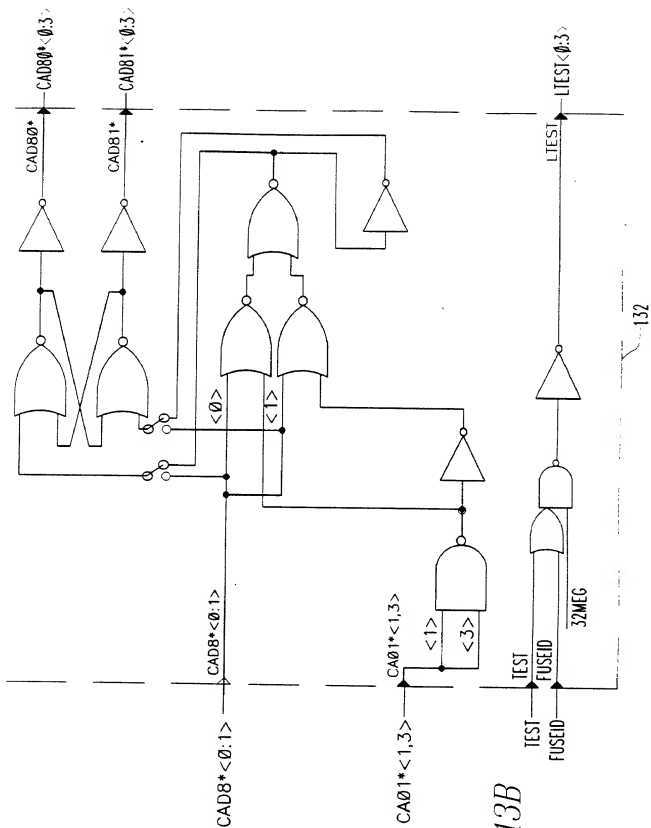


FIG. 13B



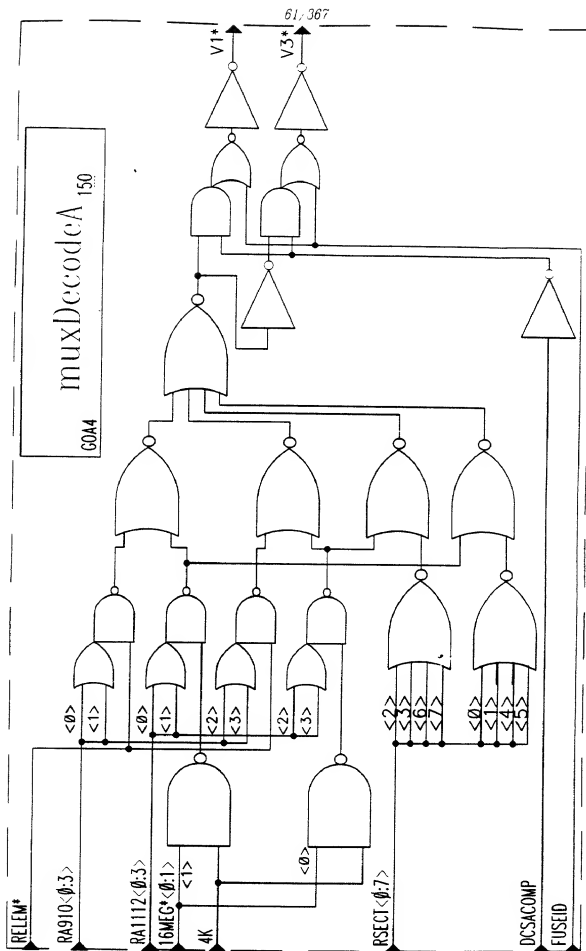


FIG. 11

FIG 15 1

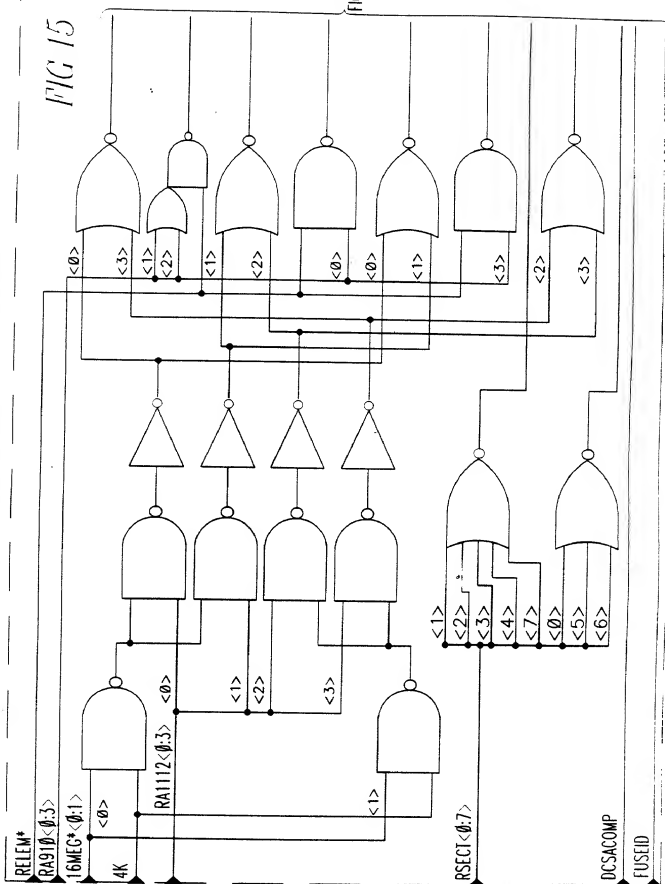


FIG. 15-2

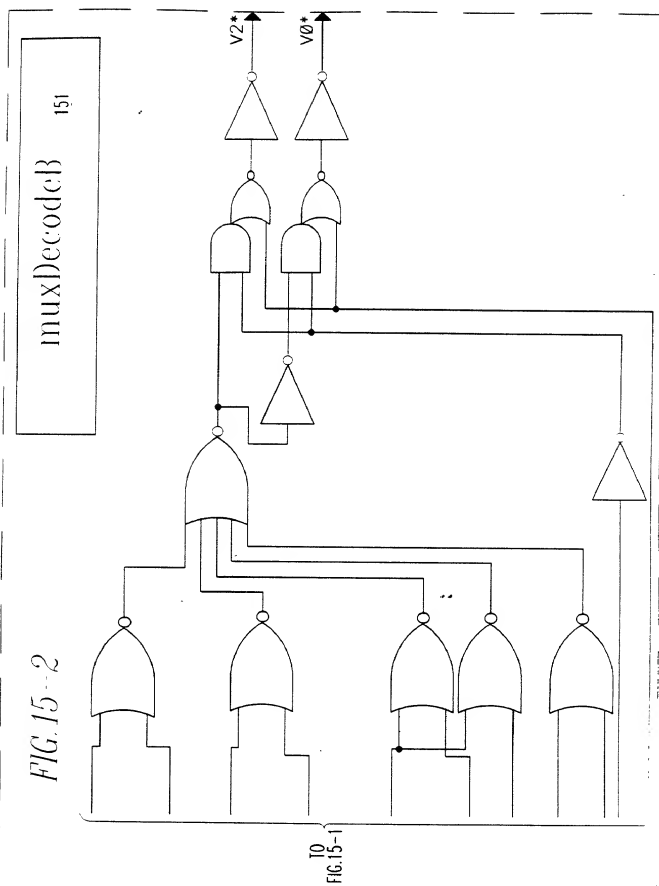
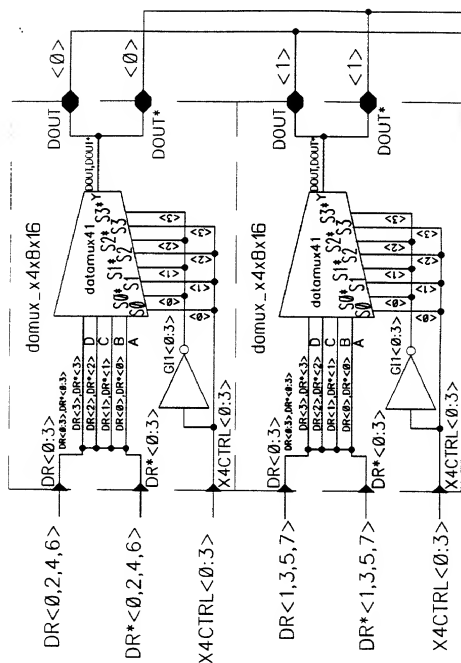
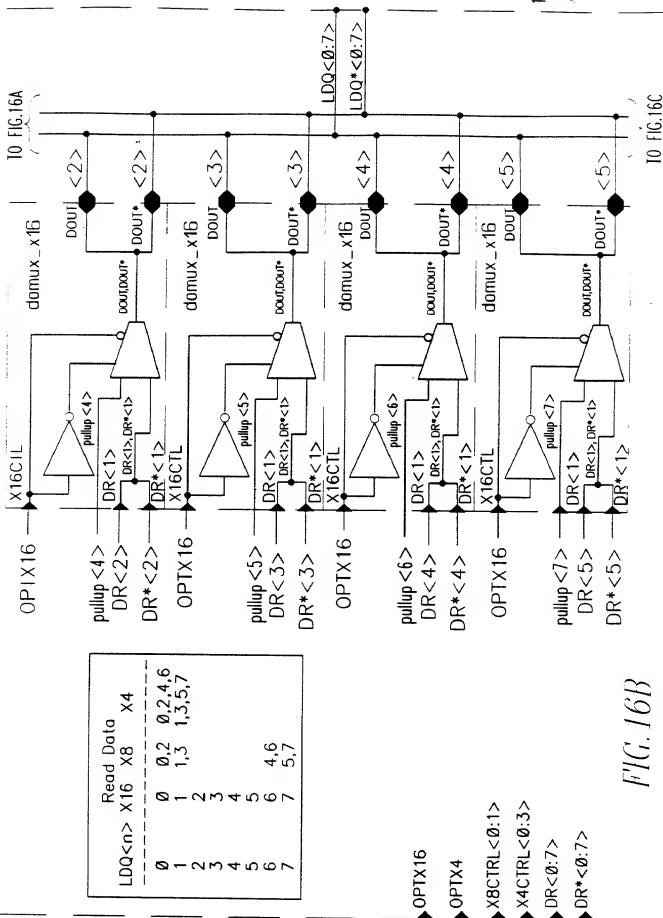


FIG. 16A



TO FIG. 16B



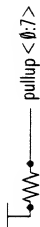


FIG. 16C

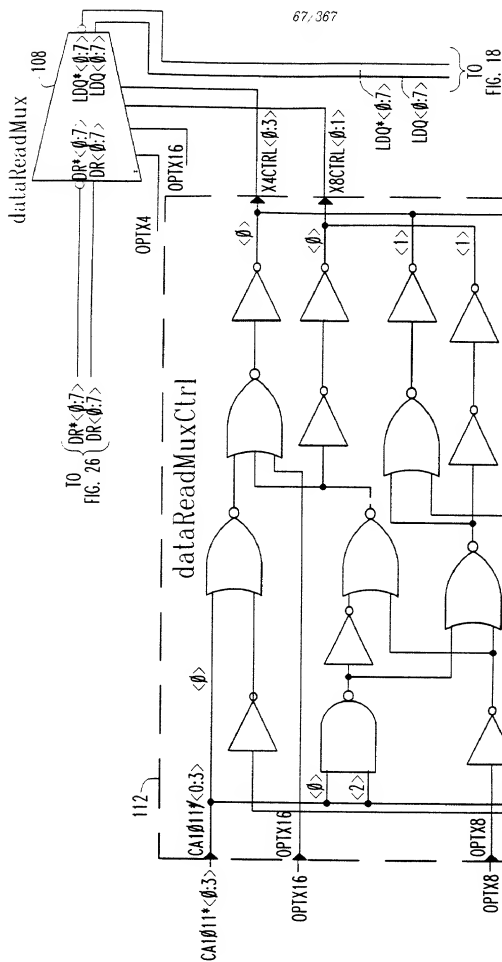


FIG. 17

## DATA OUTPUT BUFFER

110

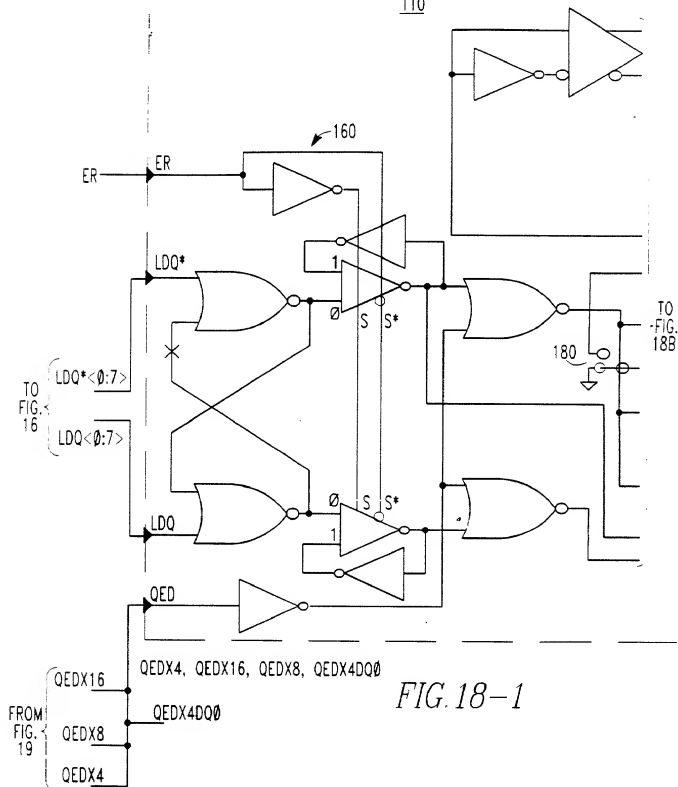


FIG. 18-1



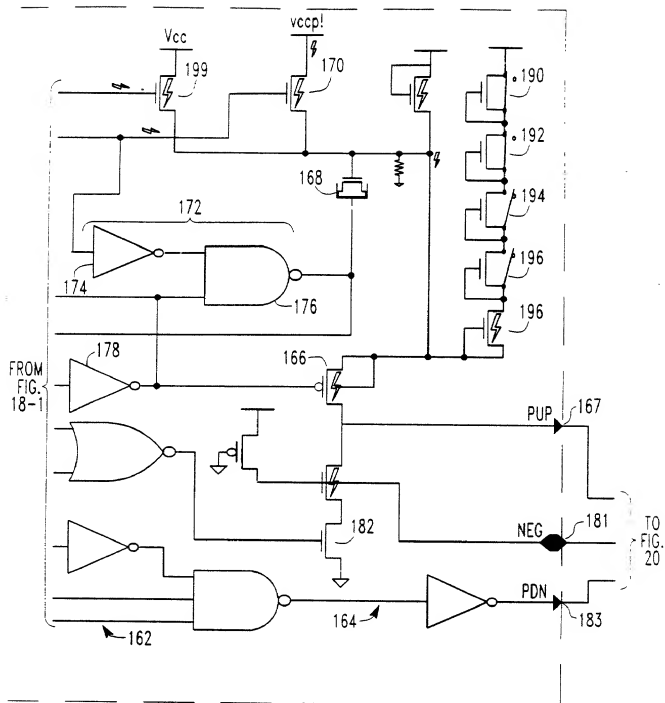


FIG. 18-2

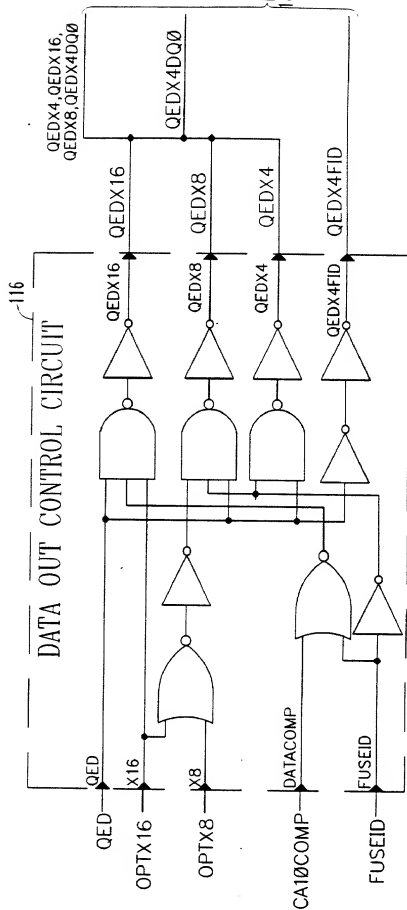


FIG. 19

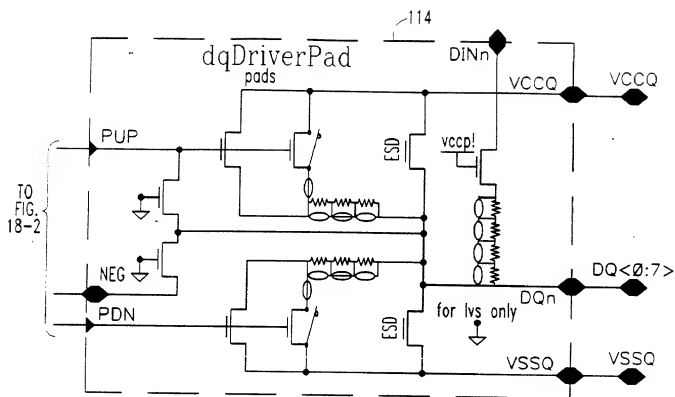


FIG. 20

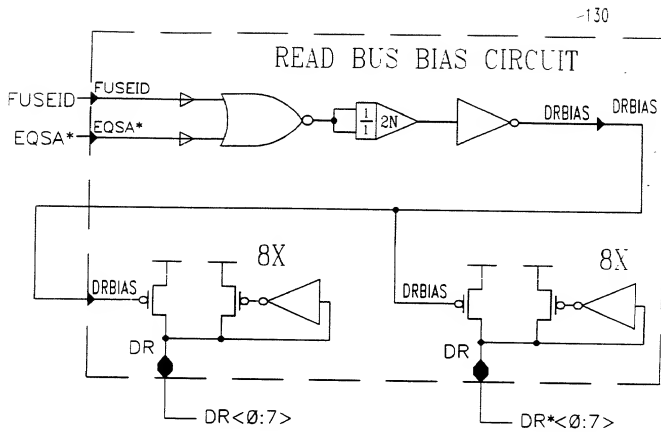


FIG. 21

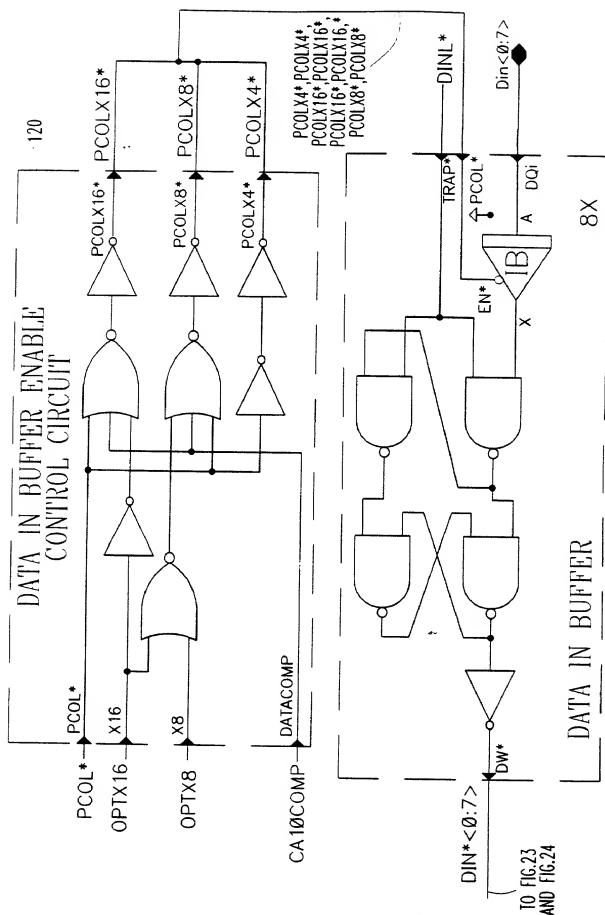
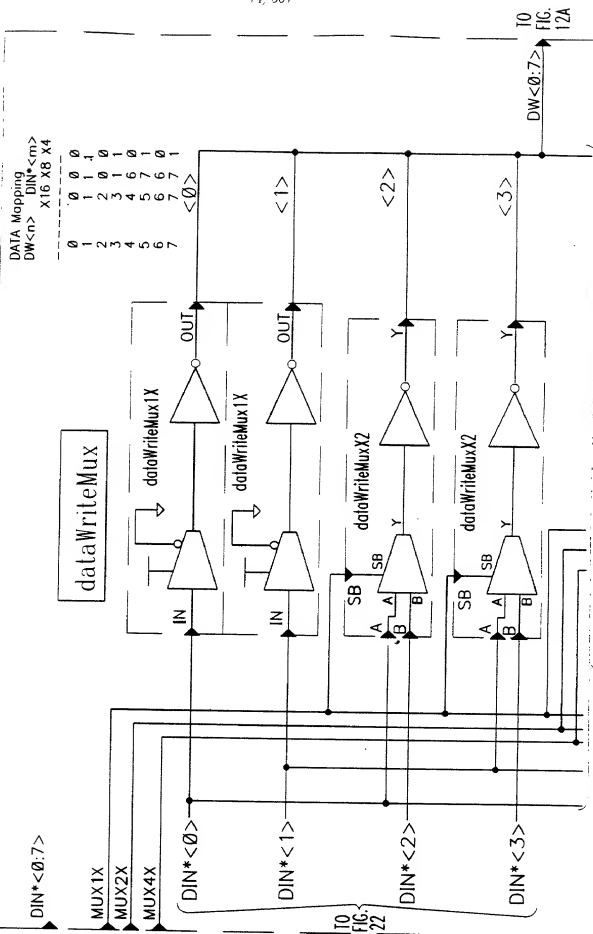


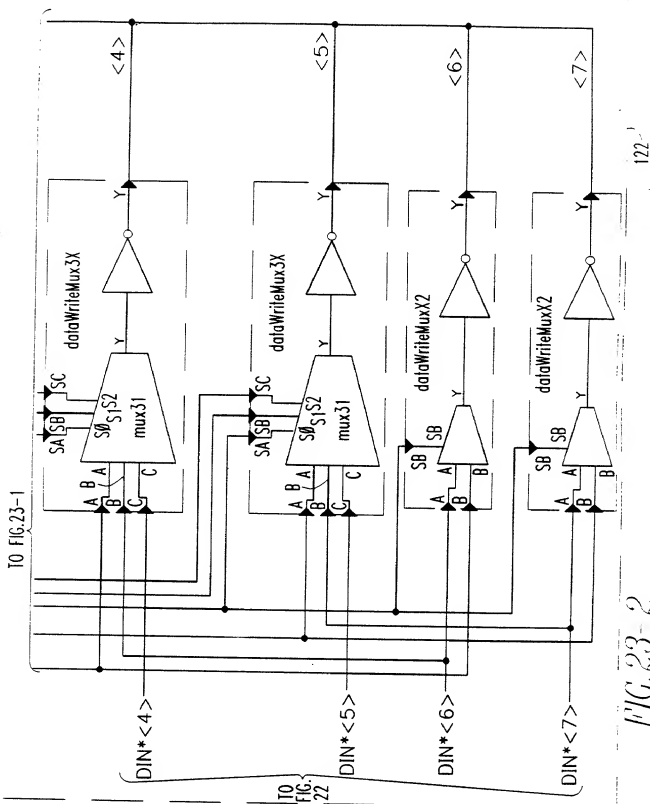
FIG. 22

FIG. 23-1

122



T0 FIG. 23-2



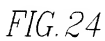


FIG. 24



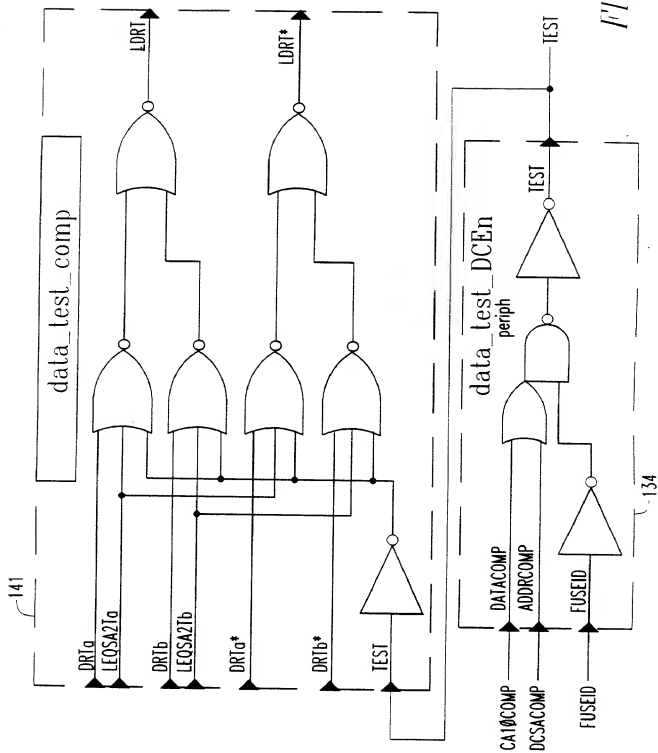


FIG. 25

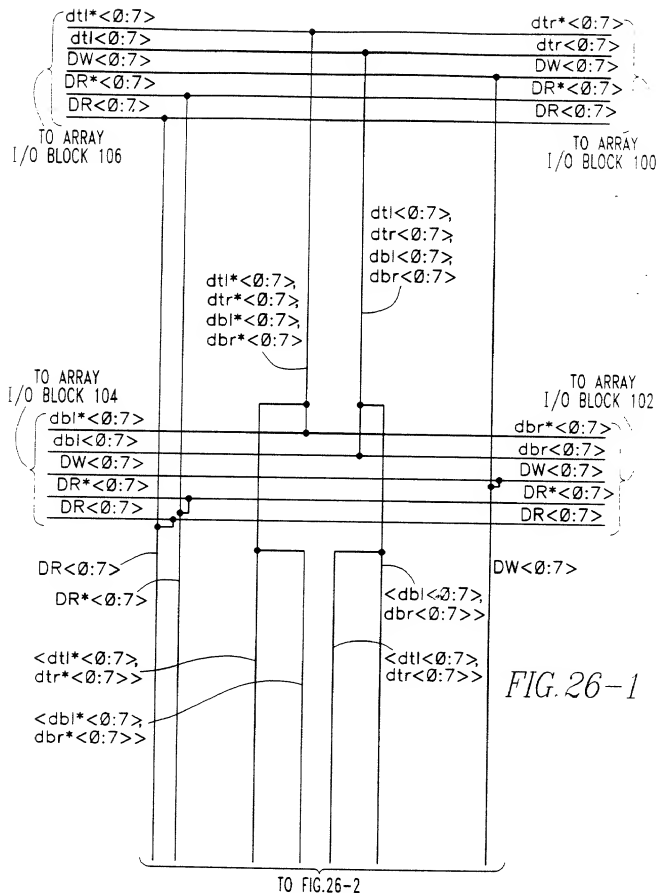


FIG. 26-1

FROM FIG.26-1

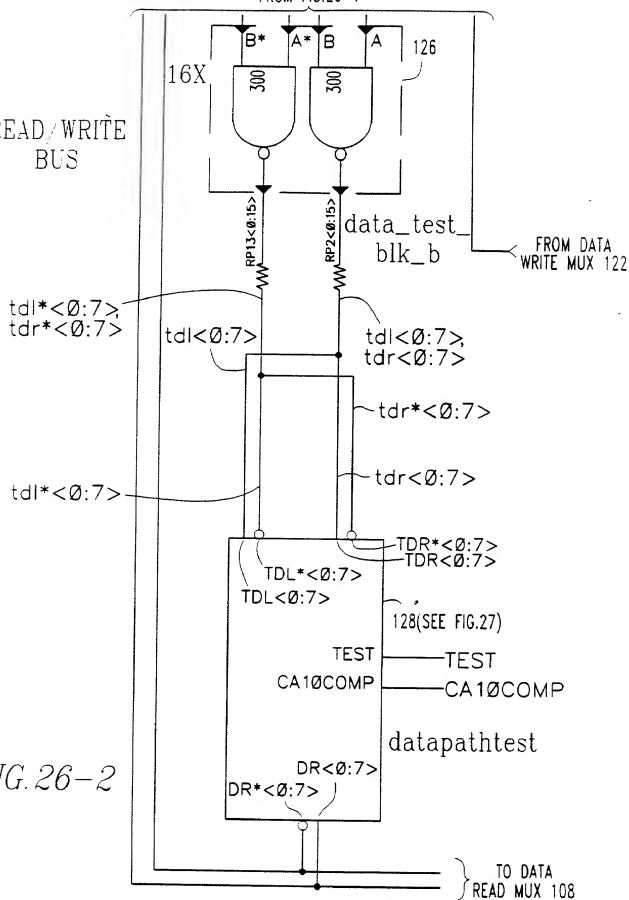
READ/WRITE  
BUS

FIG.26-2

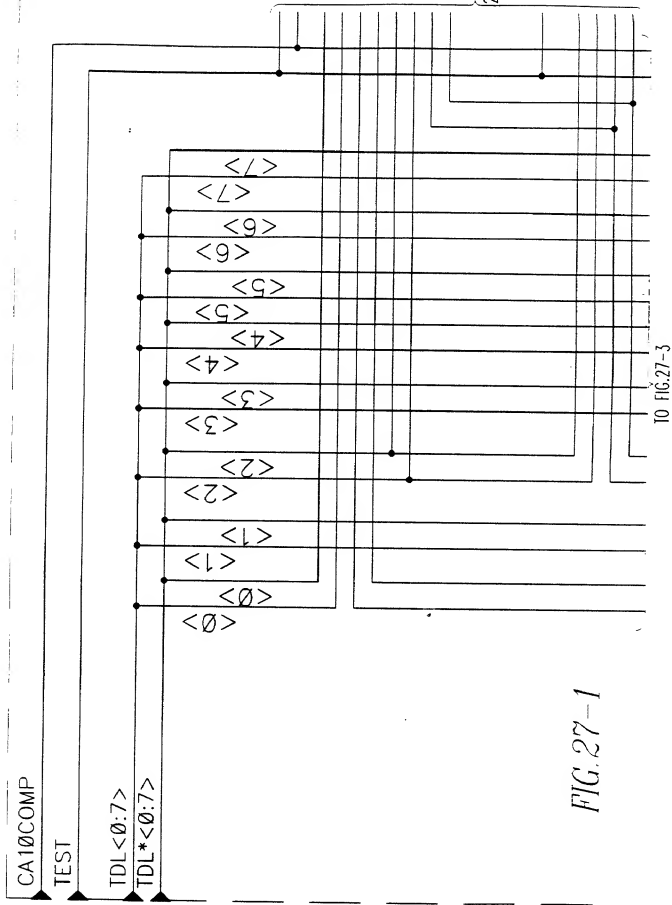
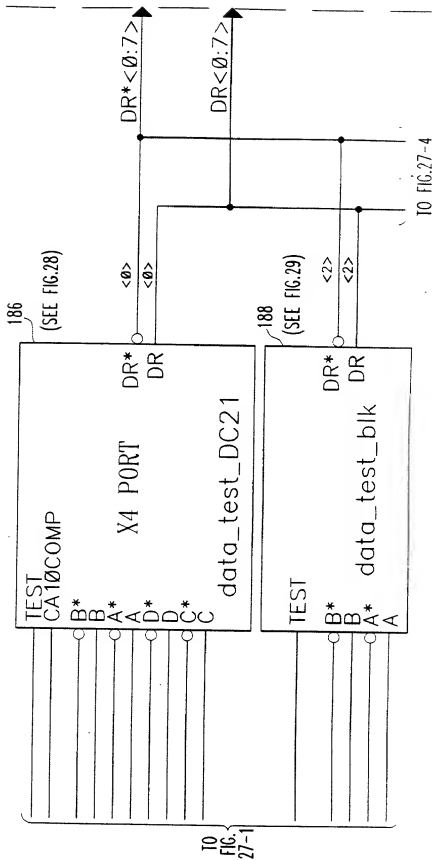


FIG. 27-1

FIG. 27-2

dataPathTest  
Block

128



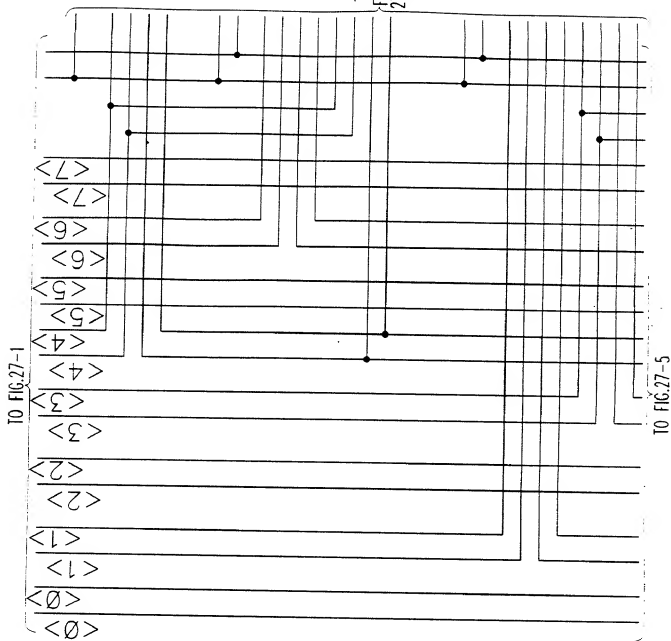
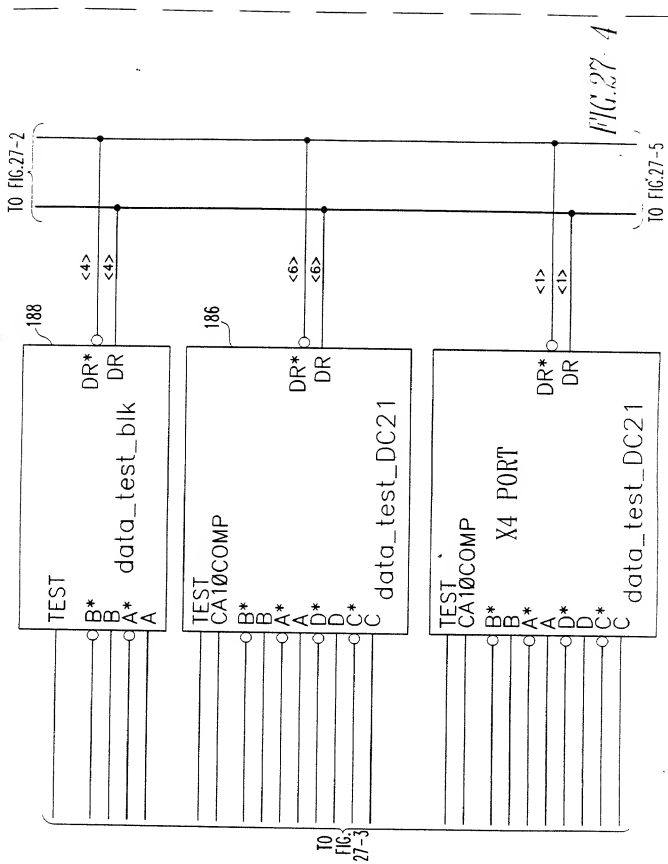


FIG. 27-3



TO FIG. 27-3

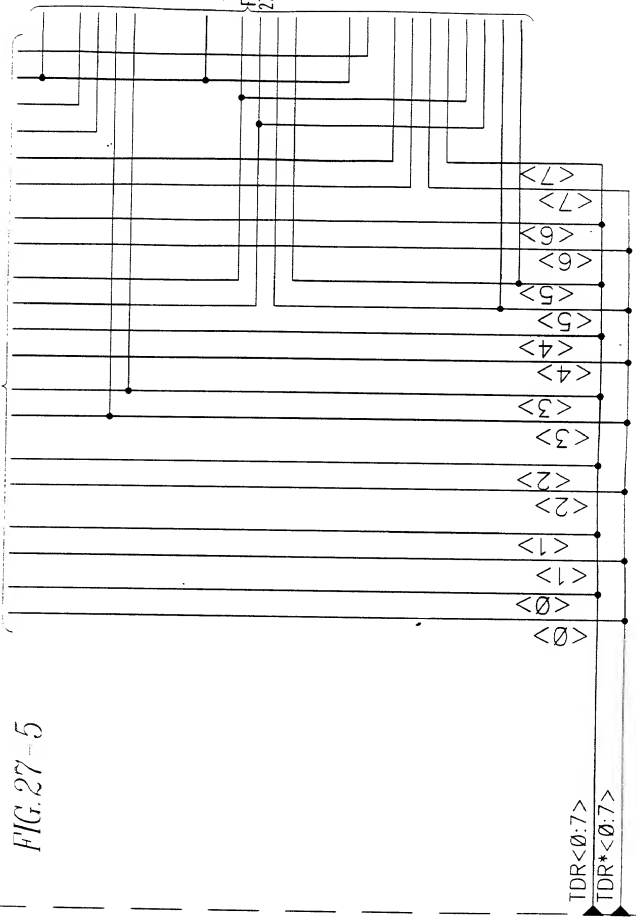
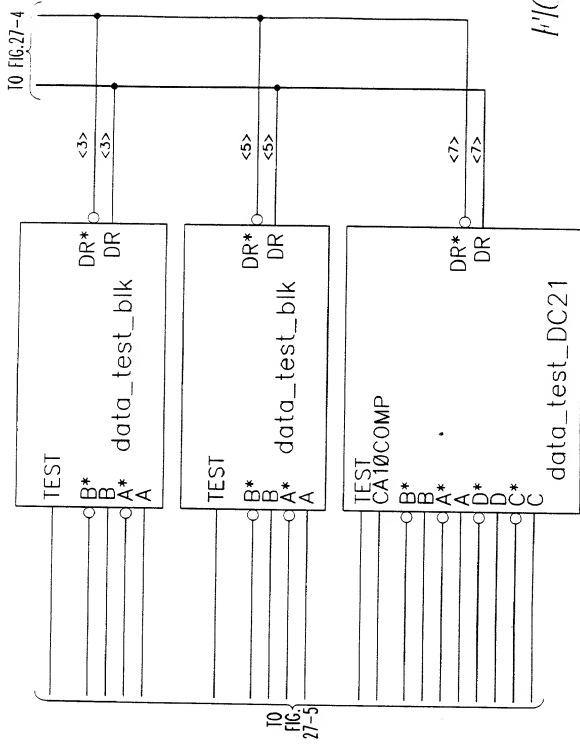


FIG. 27-6

TDR<0:7>  
TDR\*<0:7>





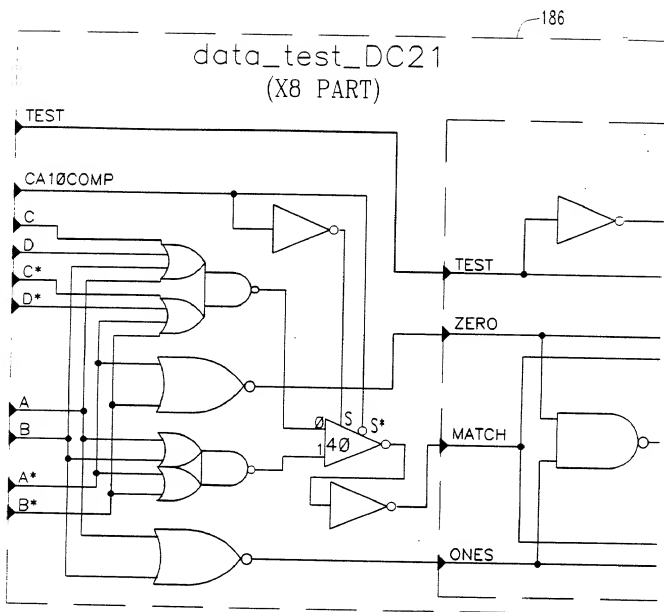


FIG. 28-1

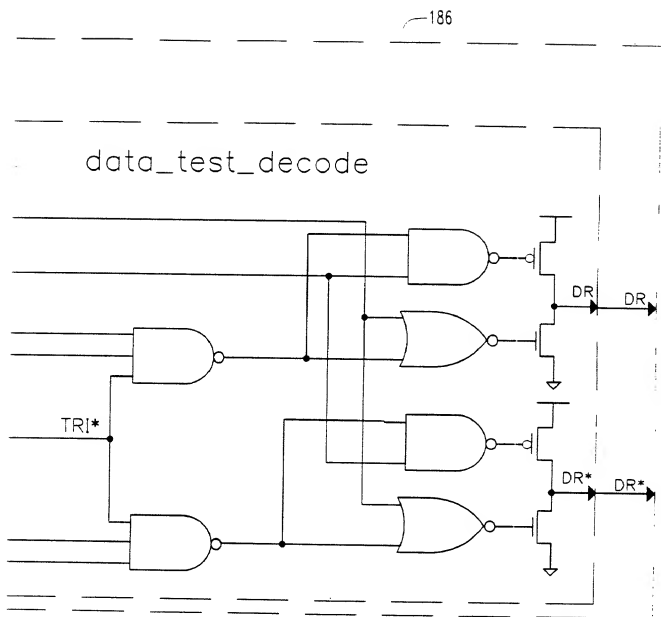


FIG. 28-2

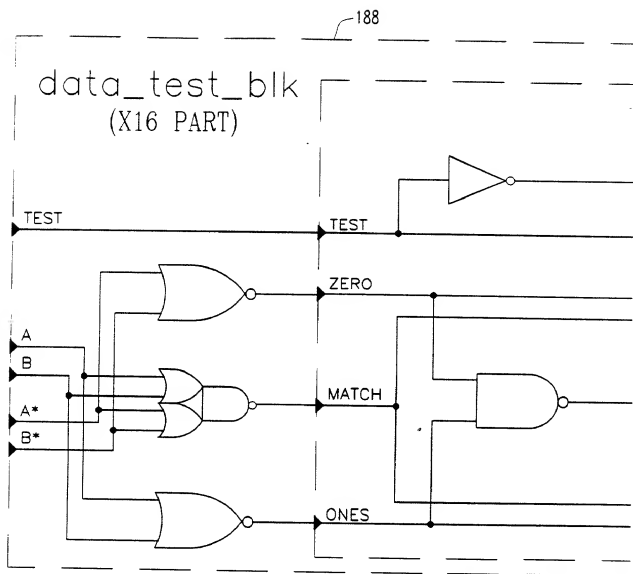


FIG. 29-1

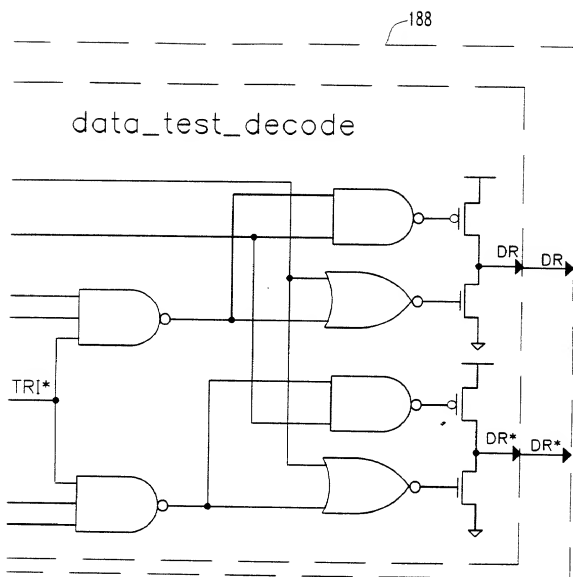


FIG. 29-2

10  
FIG. 30-2

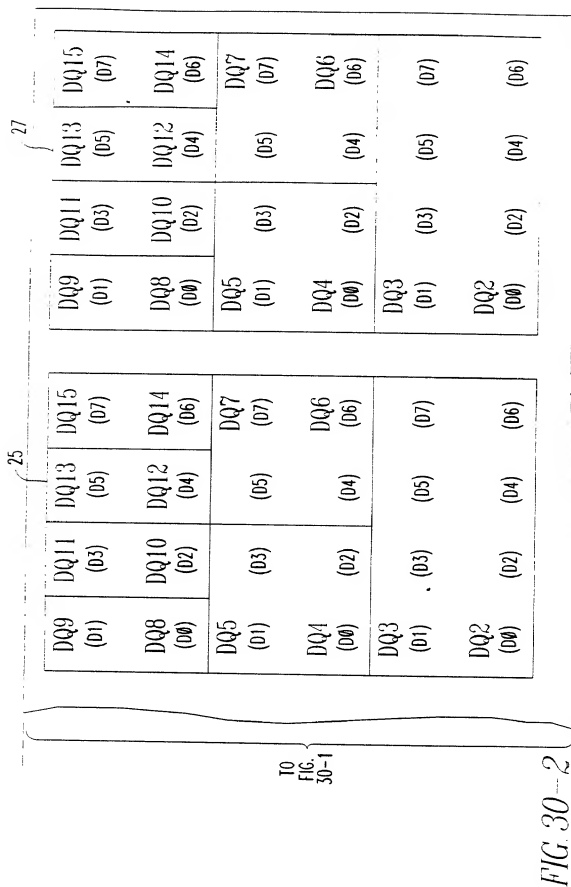
47

45

X16	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)
	DQ0 (00)	DQ2 (02)	DQ4 (04)	DQ6 (06)
	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)
X8	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)
	DQ0 (00)	DQ2 (02)	DQ4 (04)	DQ6 (06)
	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)
X4	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)
	DQ0 (00)	DQ2 (02)	DQ4 (04)	DQ6 (06)
	DQ1 (01)	DQ3 (03)	DQ5 (05)	DQ7 (07)

FIG. 30-1

10 FIG. 30-3



TO FIG. 30-4

TO FIG. 30-1

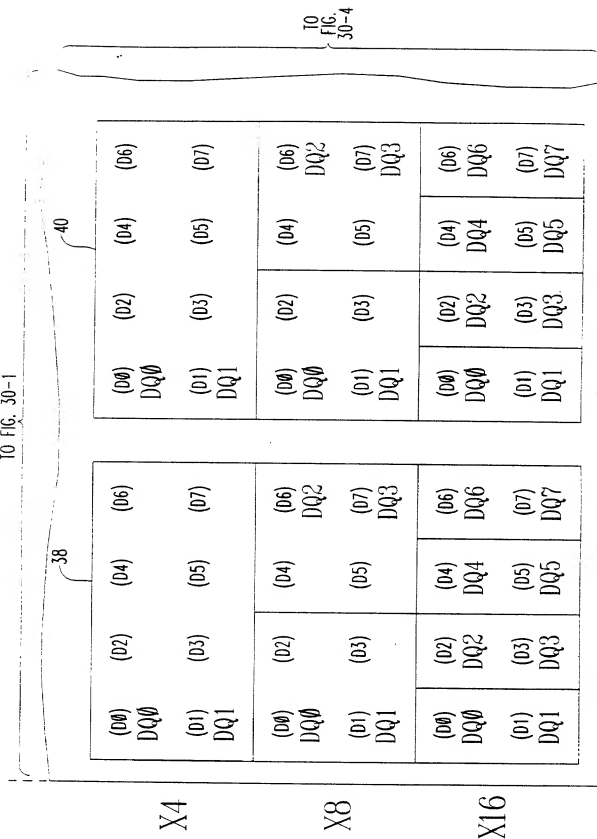


FIG. 30-3



TO FIG. 30-2

31

33

(00) DQ2	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06) DQ6
(01) DQ5	(03)	(05)	(07) DQ7
(00) DQ8	(02) DQ10	(04)	(06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

(00) DQ2	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06) DQ6
(01) DQ5	(03)	(05)	(07) DQ7
(00) DQ8	(02) DQ10	(04) DQ12	(06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

TO  
FIG.  
30-3

FIG. 30-1

<b>X4</b>	VSSQ	N/C	VSSQ	N/C	N/C						
<b>X8</b>	VSSQ	DQ3	VSSQ	DQ2	N/C						
<b>X16</b>	VSSQ	DQ7	VSSQ	DQ6	DQ5						
	1	2	3	4	5	6	7	8	9	10	11
<b>X16</b>	VCCQ	DQ0	DQ0	VCCQ	DQ1	DQ1	DQ2	VCCQ			
<b>X8</b>	VCCQ	DQ0	DQ0	VCCQ	DQ1	DQ1	N/C	N/C			
<b>X4</b>	VCCQ	DQ0	DQ0	VCCQ	DQ1	DQ1	N/C	N/C			

TO FIG. 31A2

FIG. 31A1

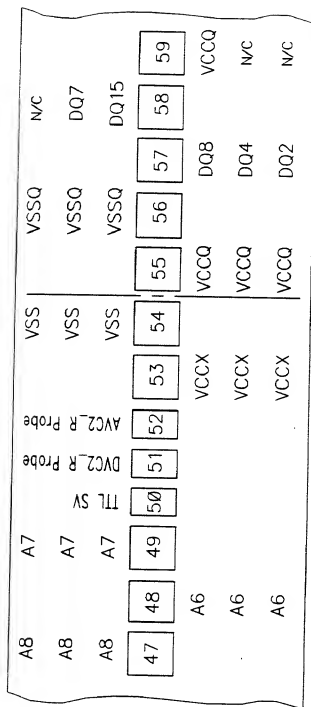
↓

[illegible]

FIG. 31A2







TO FIG. 31C2

FIG. 31C1

TO FIG. 31C1

N/C	N/C	N/C	VSSQ	N/C	VSSQ	VBB
N/C	DQ6	N/C	VSSQ	N/C	VSSQ	VBB
VSSQ	DQ14	DQ13	VSSQ	DQ12	VSSQ	VBB
60	61	63	64	65	66	67
	62	63	64	65	66	67
DQ9		DQ10	VCCQ	DQ11	VCCQ	VBB
DQ5		N/C	VCCQ	N/C	VCCQ	VBB
DQ3		N/C	VCCQ	N/C	VCCQ	VBB

FIG. 31C2





TO  
FIG.  
32A3

PART TYPE	32MEG
ANY 16K	RA 13
X4 8K OR 4K	CA 12
X8 8K OR 4K	CA 11
X16 8K OR 4K	CA 10

FIG. 32A2

CA 6-0:1 > MSB  
 CA45-0:3 >  
 CA23-0:3 >  
 CA01-0:3 >  
 CA 8-0:1 > LSB

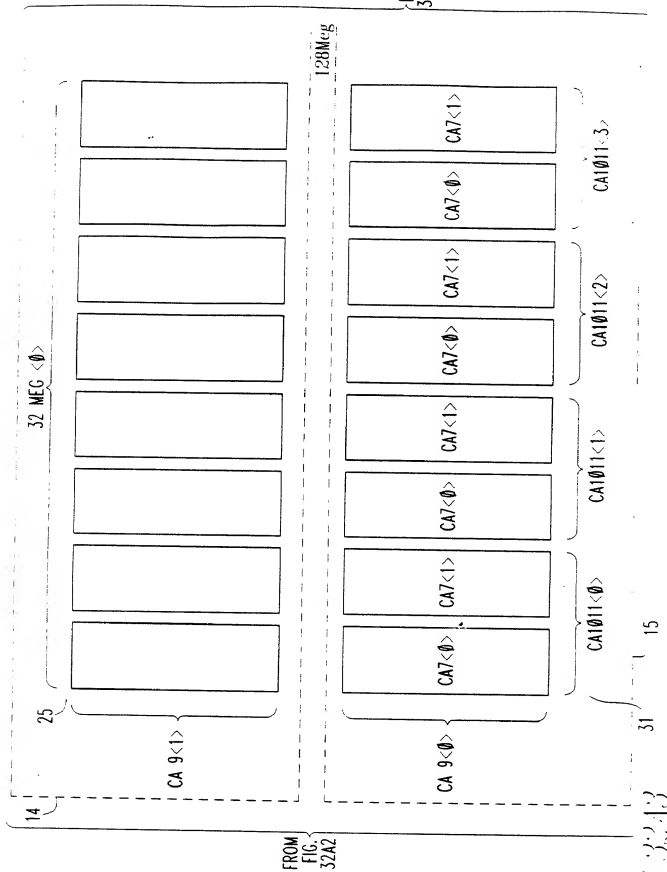
32 MEG &lt;1&gt; (8K)

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FROM  
FIG.  
32A1

LSB → MSB

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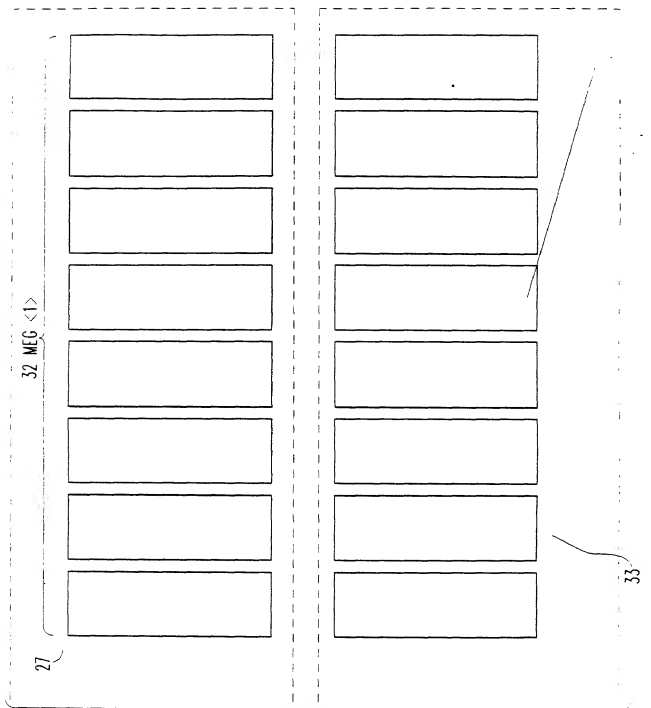
FROM  
FIG.  
32A3

FIG. 32A4

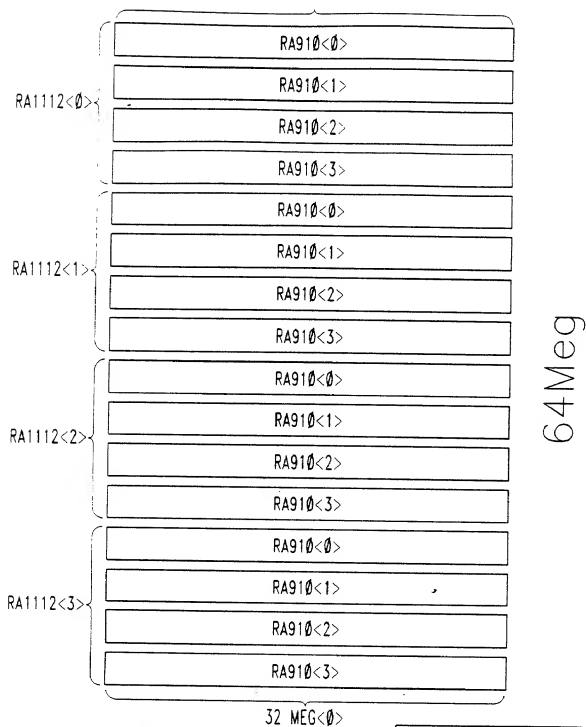


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

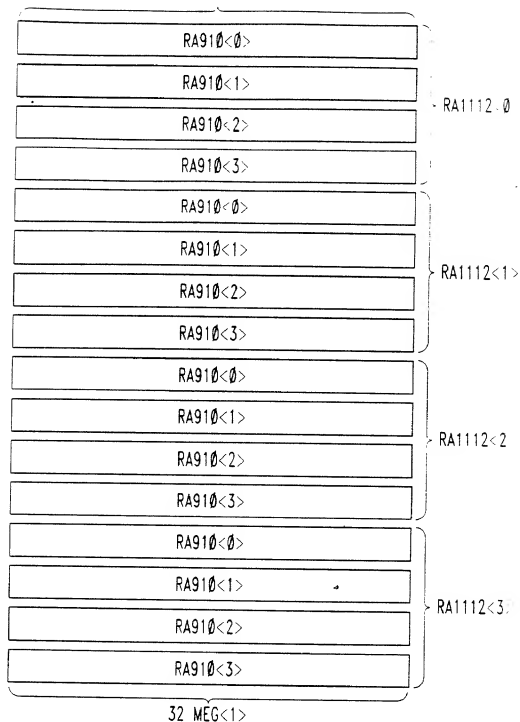
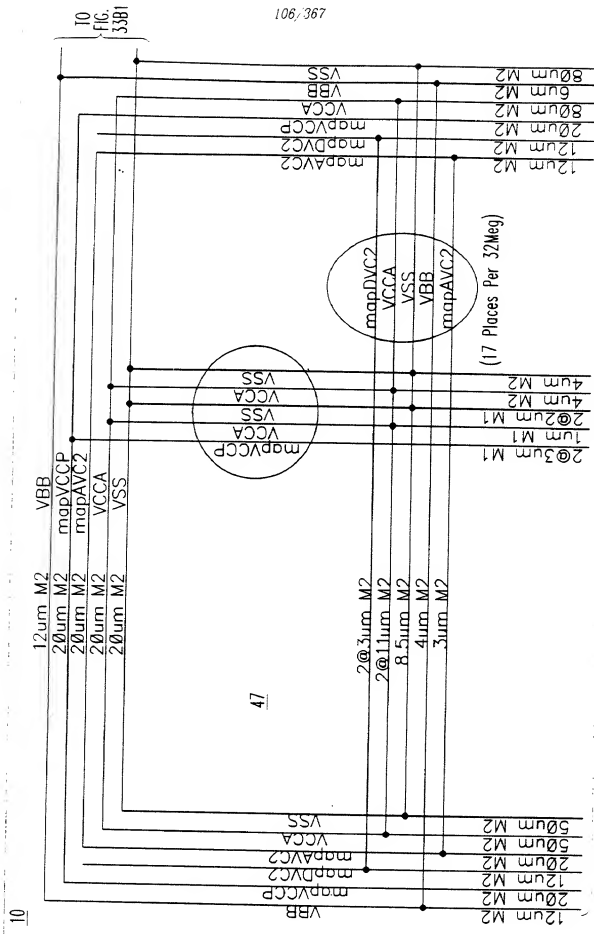


FIG. 32B2

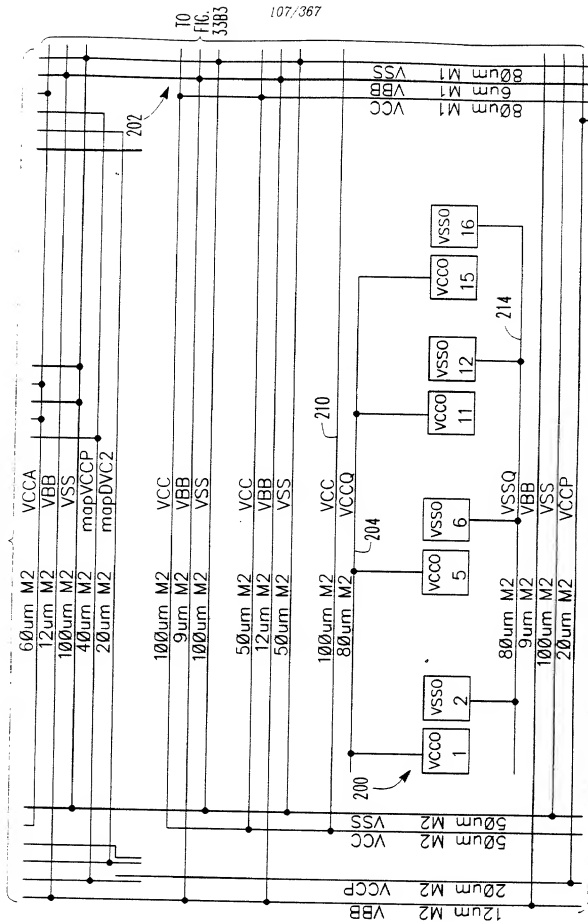
FIG. 33A



TO FIG. 33A2

FIG. 33A1

FROM FIG. 33A1



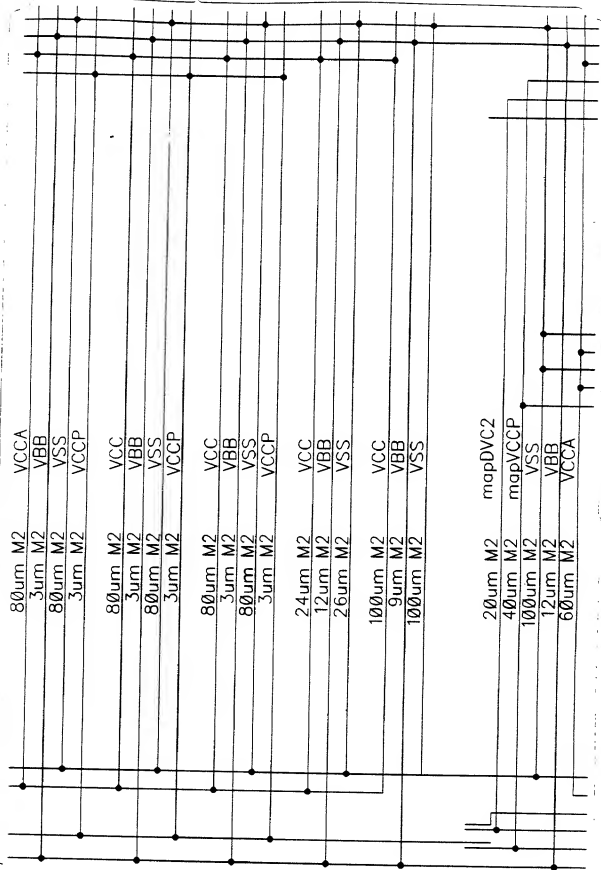
TO  
FIG.  
33B3

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TO FIG. 33A3

FIG. 33A2

FROM FIG. 33A2

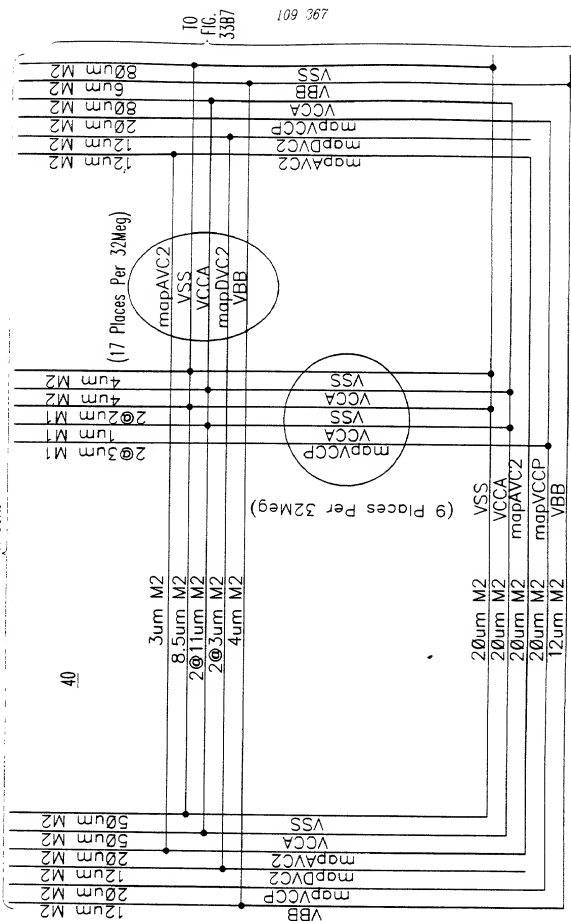


TO FIG. 33A4

FIG. 33A3



FROM FIG. 33A3



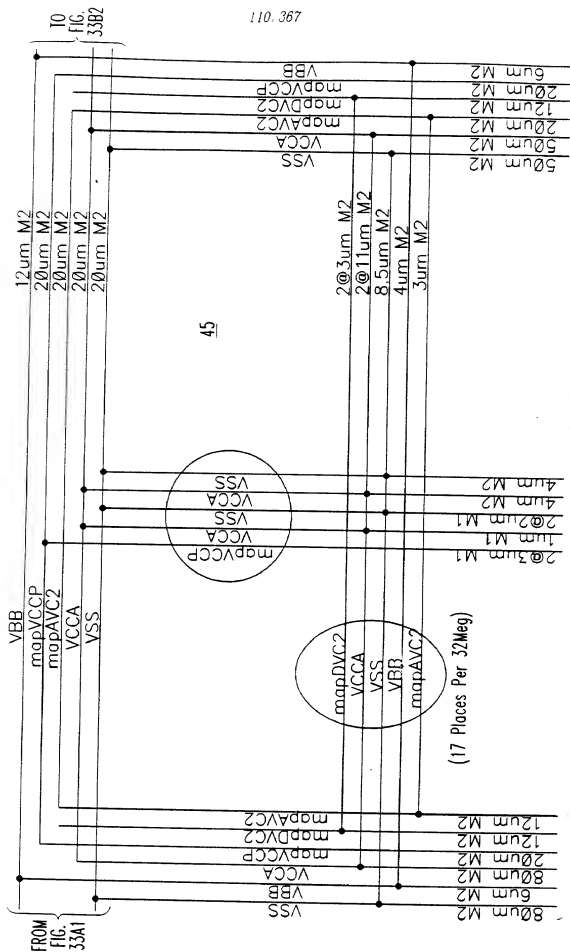


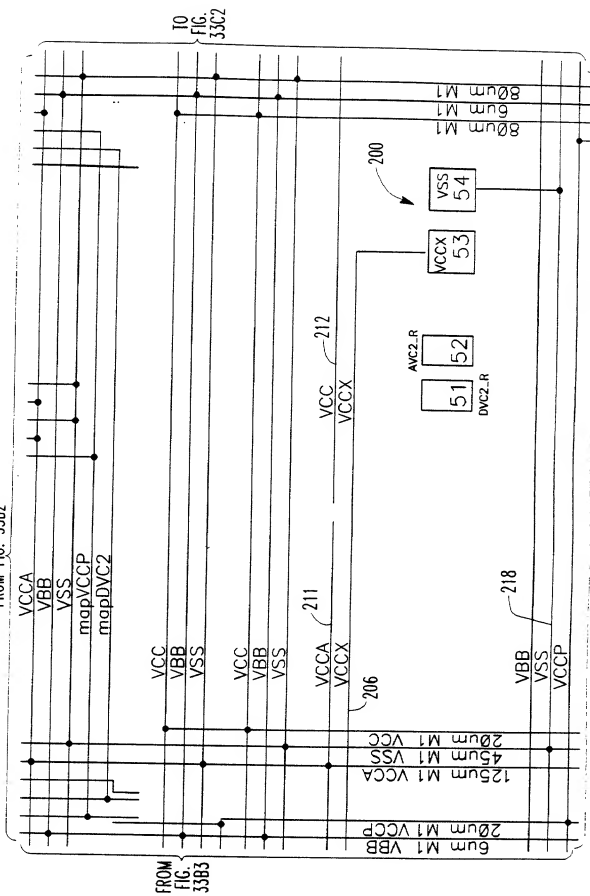
FIG. 3381





TO FIG. 3383

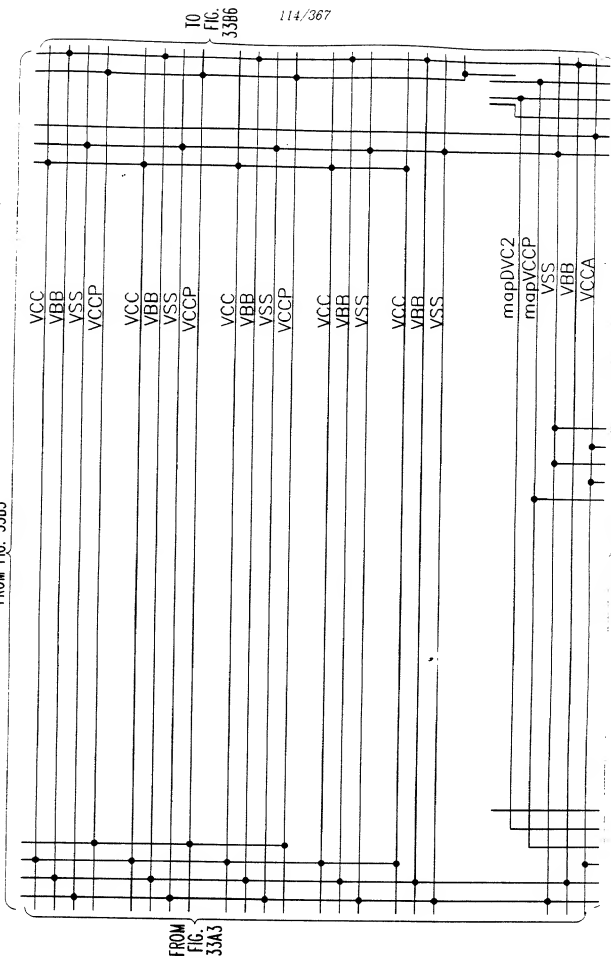
FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B1

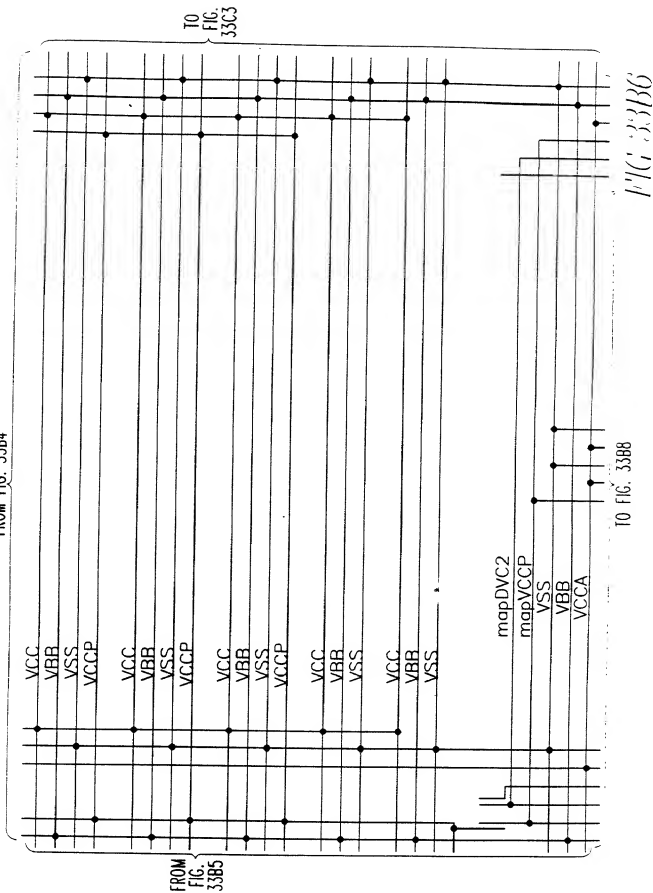
FROM FIG. 33B3



TO FIG. 33B7

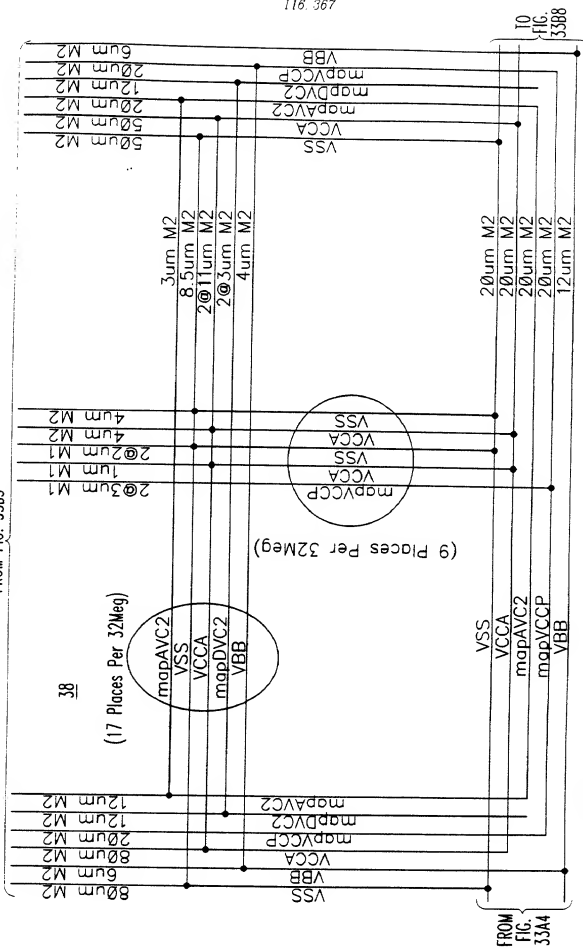
FIG. 33B5

FROM FIG. 33B4



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(17 Places Per 32Meg)



1716:3337



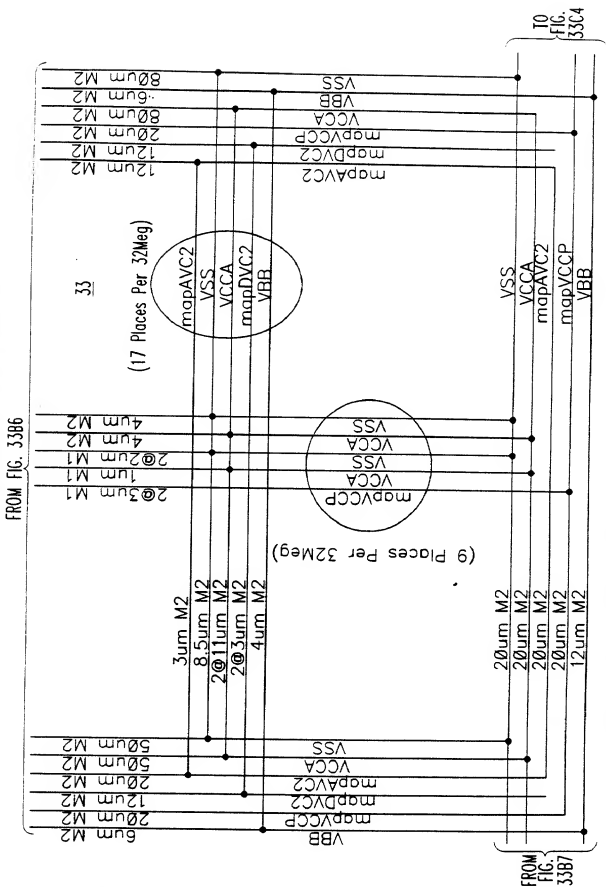
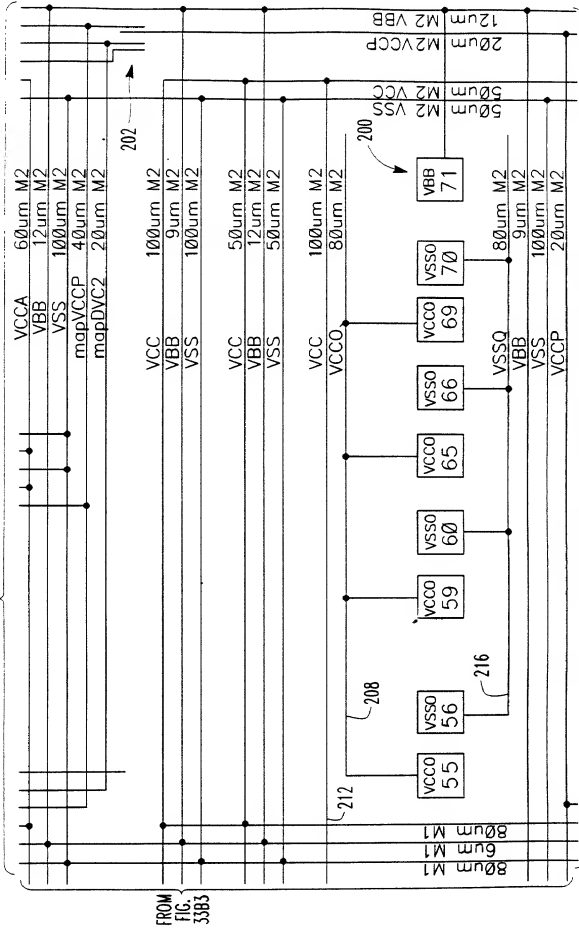


FIG. 3388



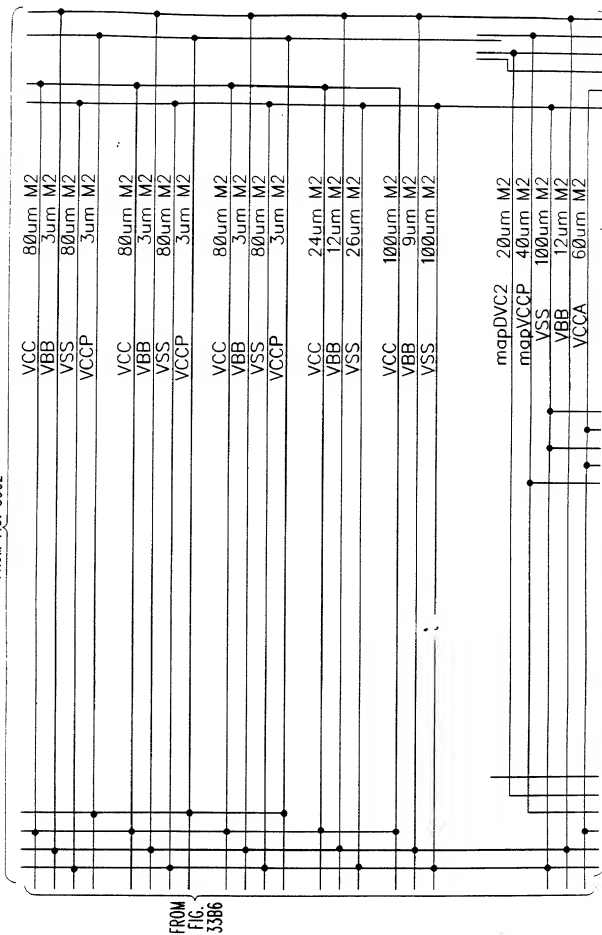
FROM FIG. 33C1

FROM  
FIG.  
33B3

TO FIG. 33C3

FIG. 33C2

FROM FIG. 33C2

FROM  
FIG. 33B6

TO FIG. 33C4

P/C 33C3



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10

45

200

TO  
FIG.  
33D3

TO FIG. 33D2

DVC2  
GENERATOR 500

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP  
PUMP CIRCUITS 402

DVC2  
GENERATOR 501

FIG. 33D1

TO FIG. 33D1

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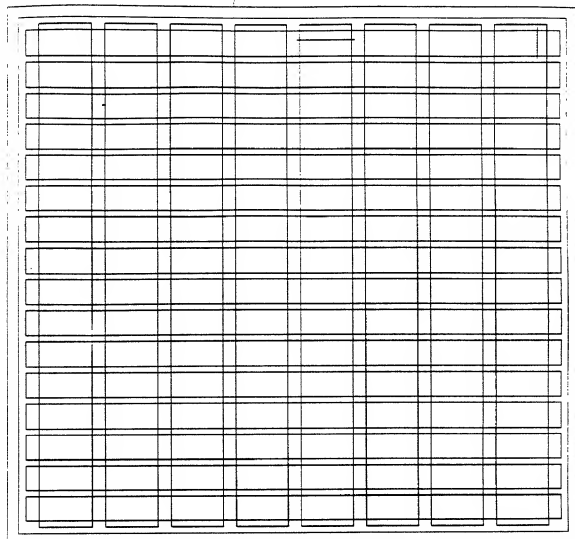
502 DVC2  
GENERATOR401 VCCP  
PUMP CONTROL503 DVC2  
GENERATORTO  
FIG.  
33D4

FIG. 33D2

TO  
FIG.  
33D1

(SEE FIG. 33E1)

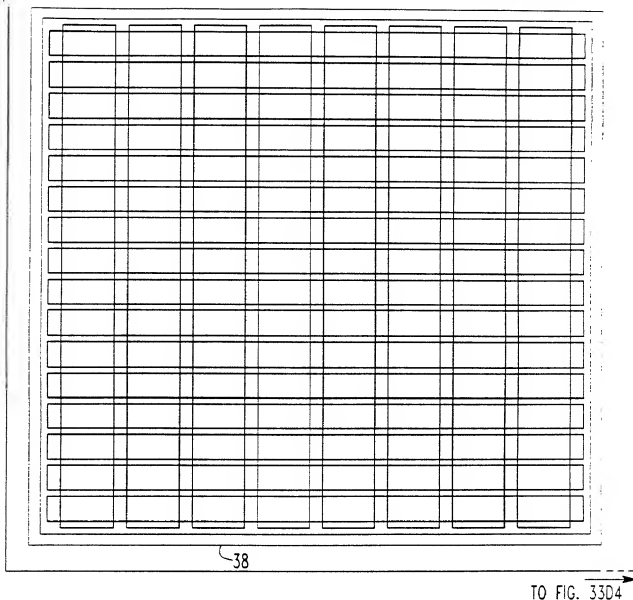
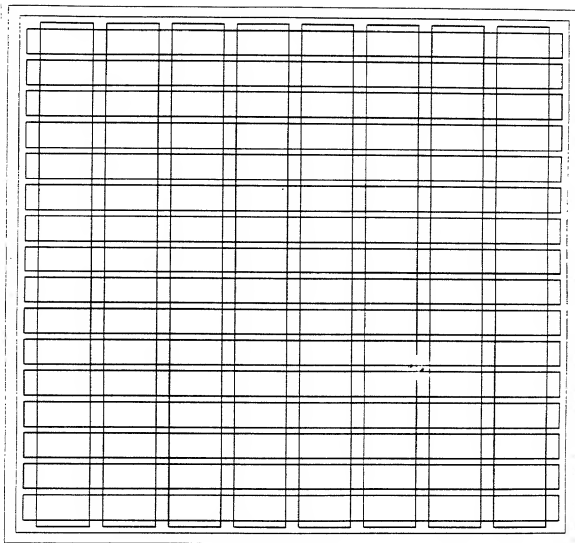


FIG. 33D3

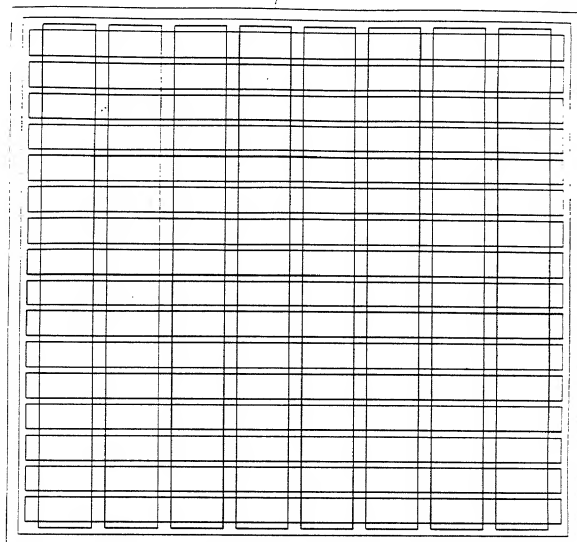


TO  
FIG.  
33D2

40

TO FIG. 33D3

FIG. 33D4



DVC2  
GENERATOR 504

□ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □

VCCP  
REGULATOR 220

DVC2  
GENERATOR 505

TO  
FIG.  
33E3

FIG. 33E1

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TO FIG. 33E1

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10

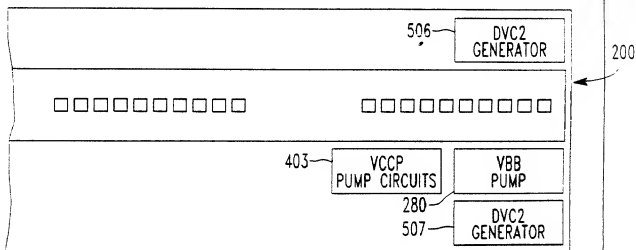
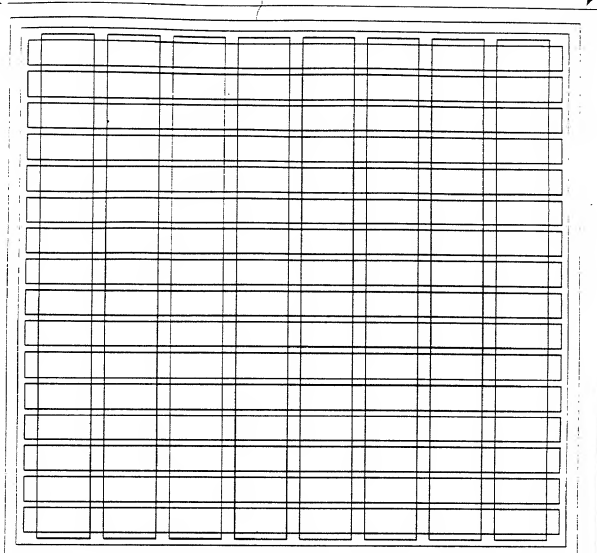
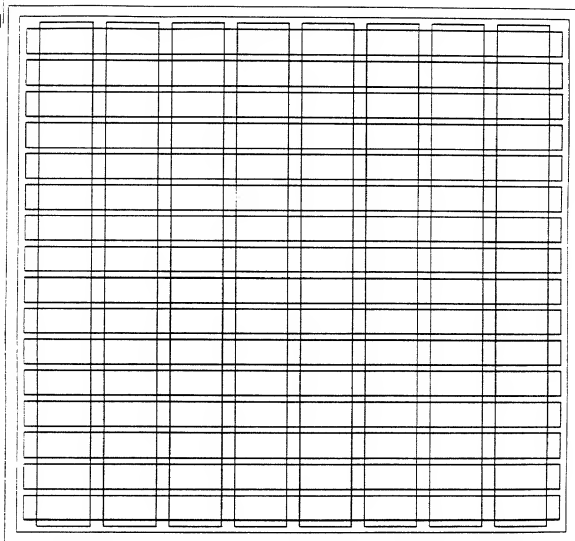


FIG. 33E2

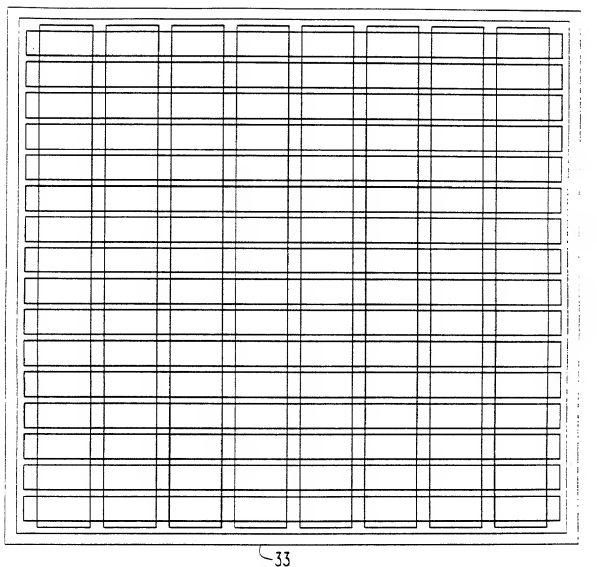
TO FIG. 33E4

TO  
FIG.  
33E1

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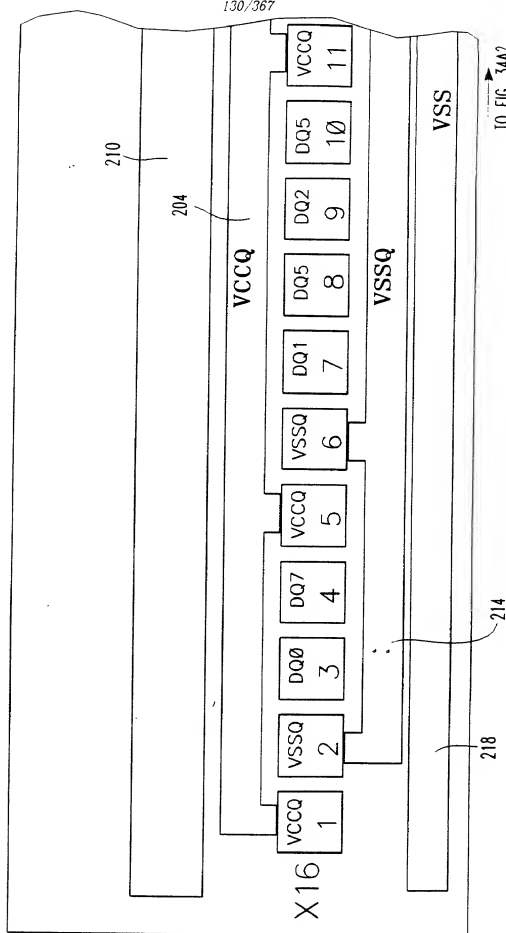
TO FIG. 33E4

FIG. 33E3



TO FIG. 33E3

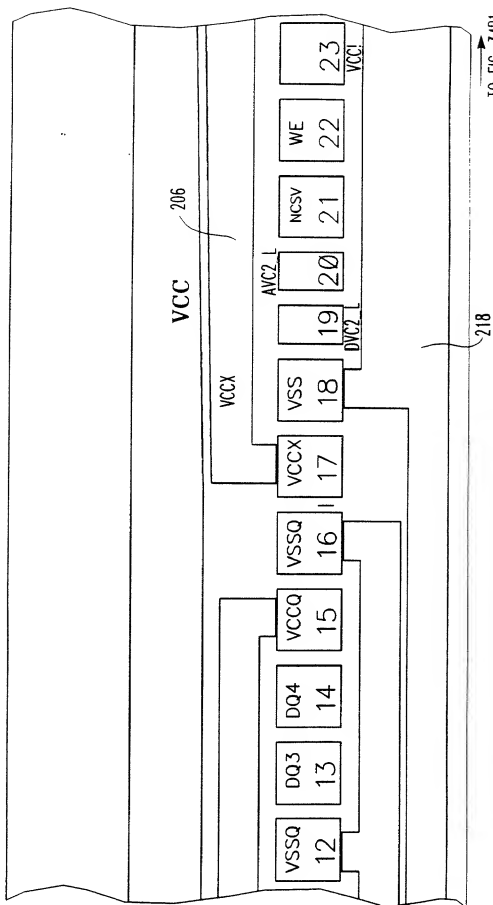
FIG. 33E4



10 FIG. 34A2

FIG. 34A1

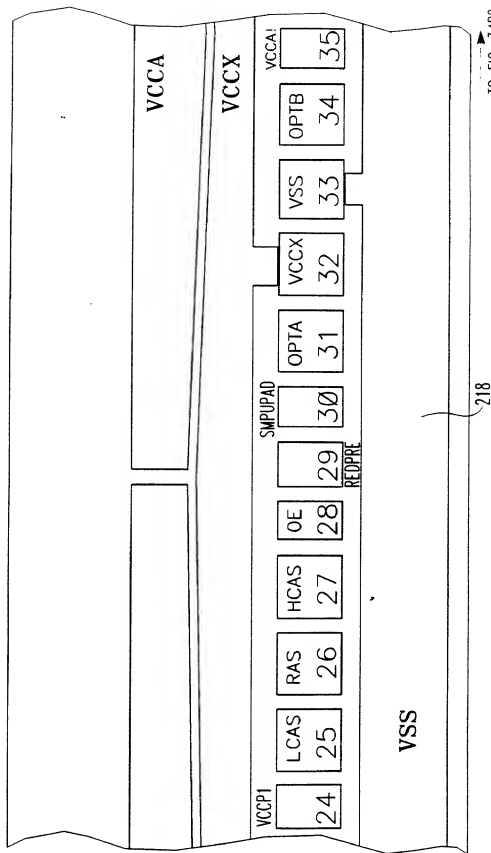
TO FIG. 34A1



TO FIG. 34B1

FIG. 34A2

TO FIG. 34A2

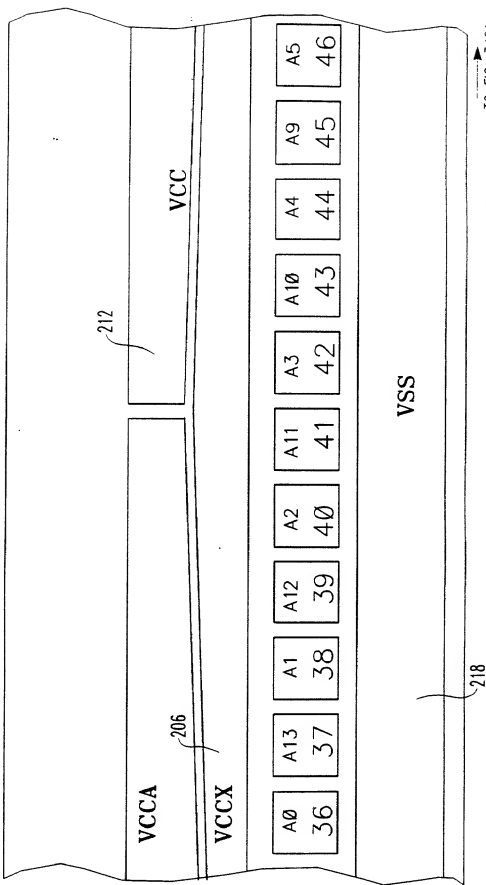


TO FIG. 34B2

FIG. 34B1



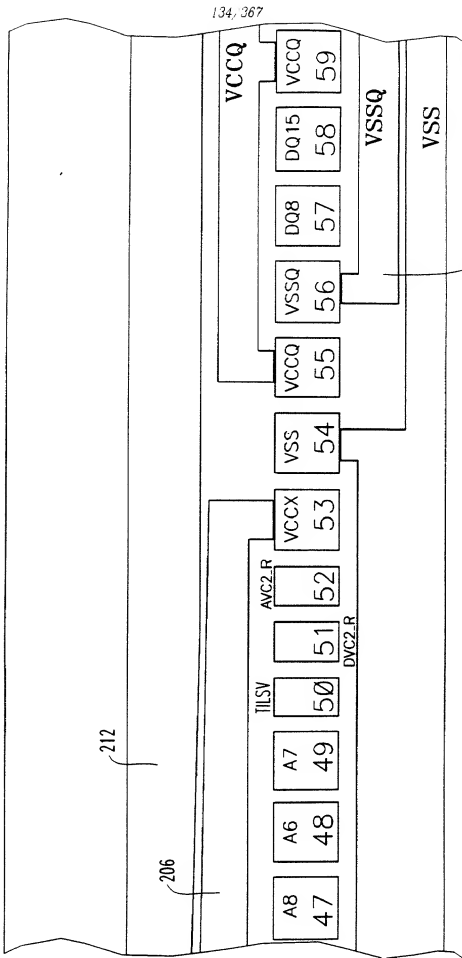
TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2



TO FIG. 34C2

FIG. 34C1

TO FIG. 34C1

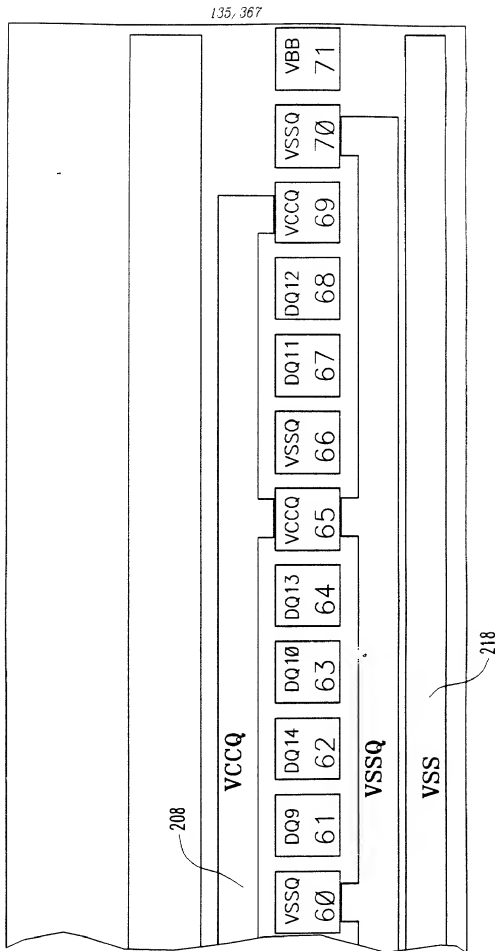


FIG. 34C2

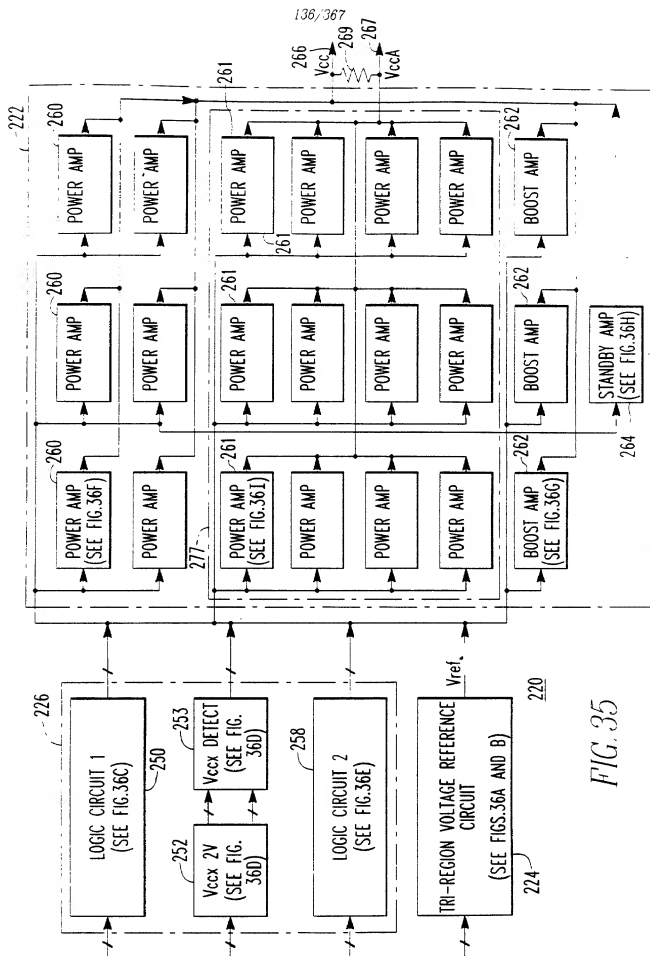


FIG. 35

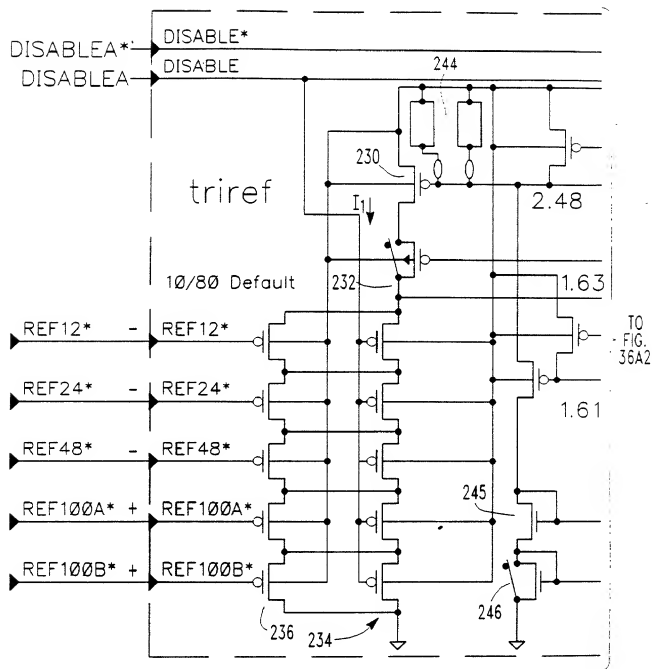


FIG. 36A1

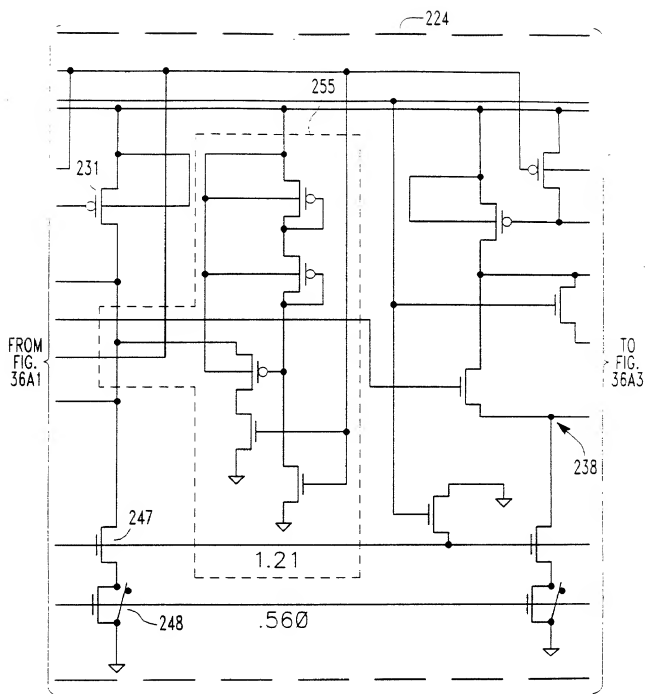


FIG. 36A2

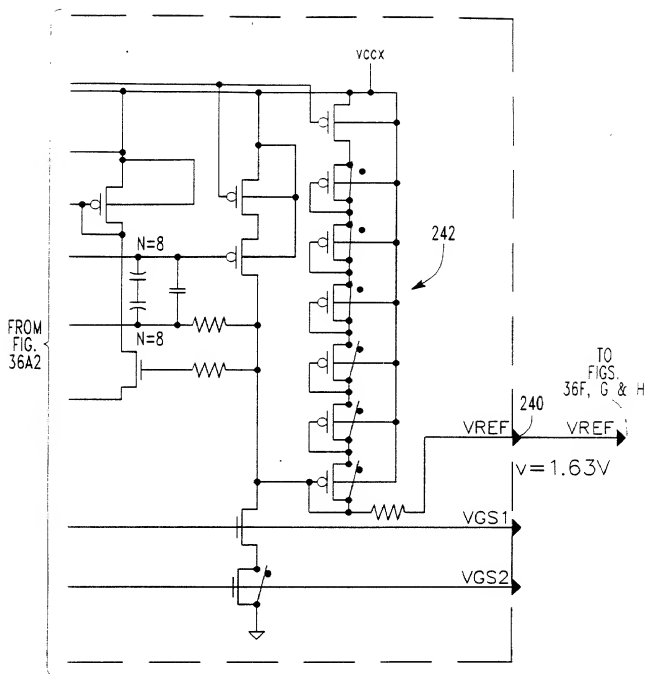


FIG. 36A3

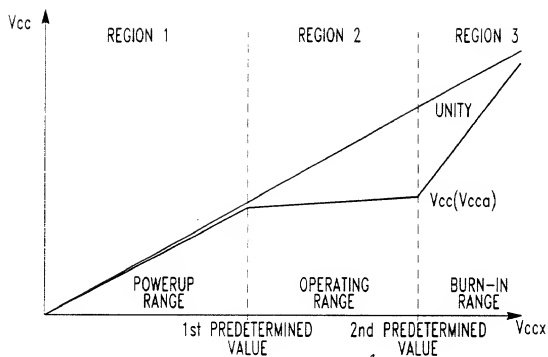


FIG. 36B



LLOW

EQ\*

RL\*

DISABLEA

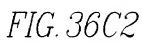
PWRUP

8KREF

ACT

TO  
FIG.  
36C2

FIG. 36C1



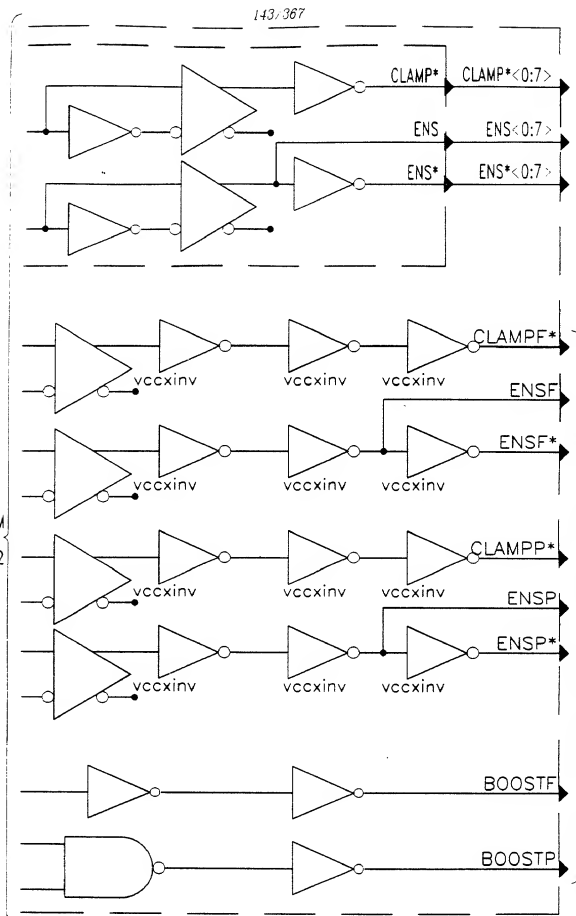
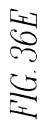
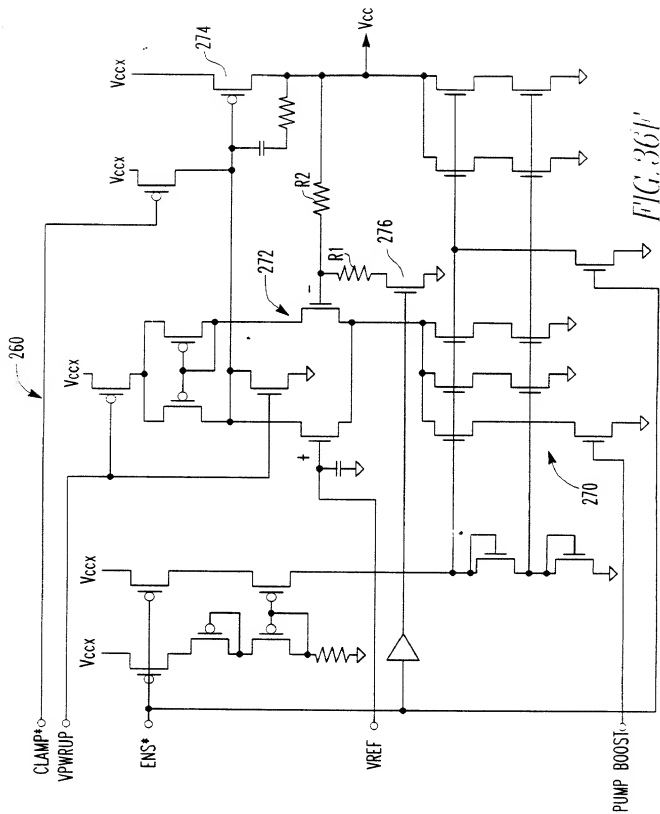
FROM  
FIG.  
36C2TO  
FIG.  
36F

FIG. 36C3







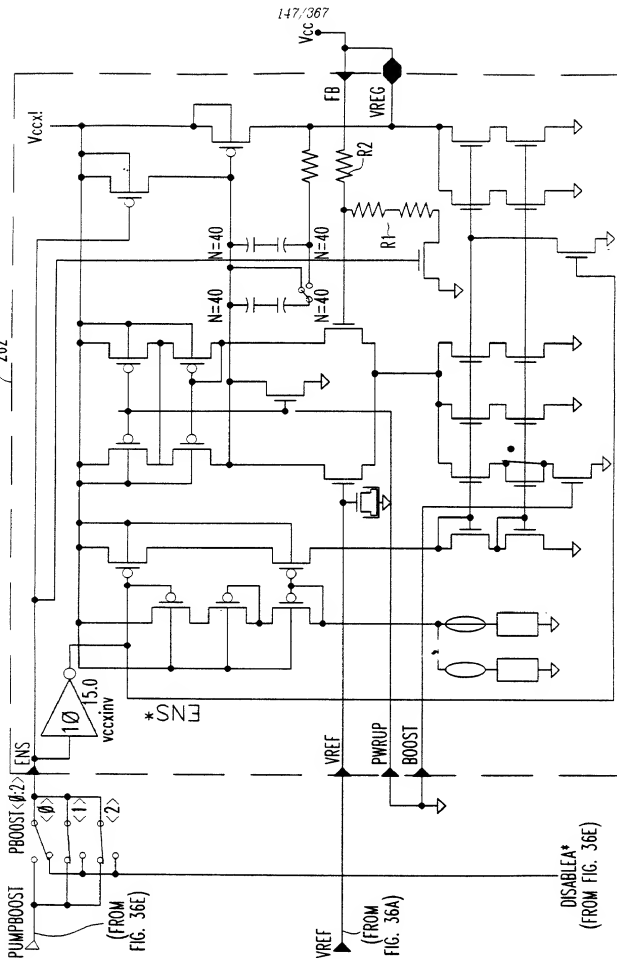
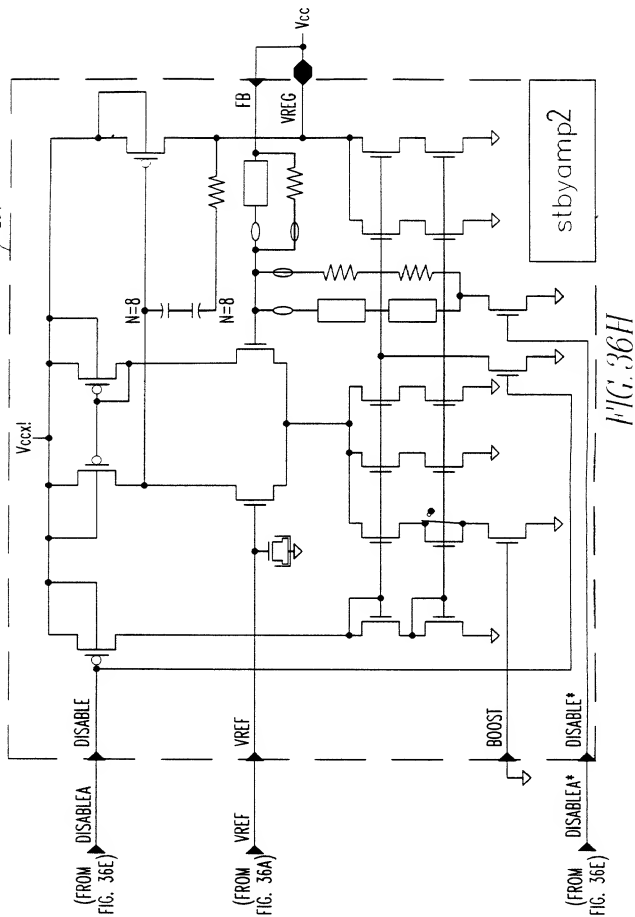


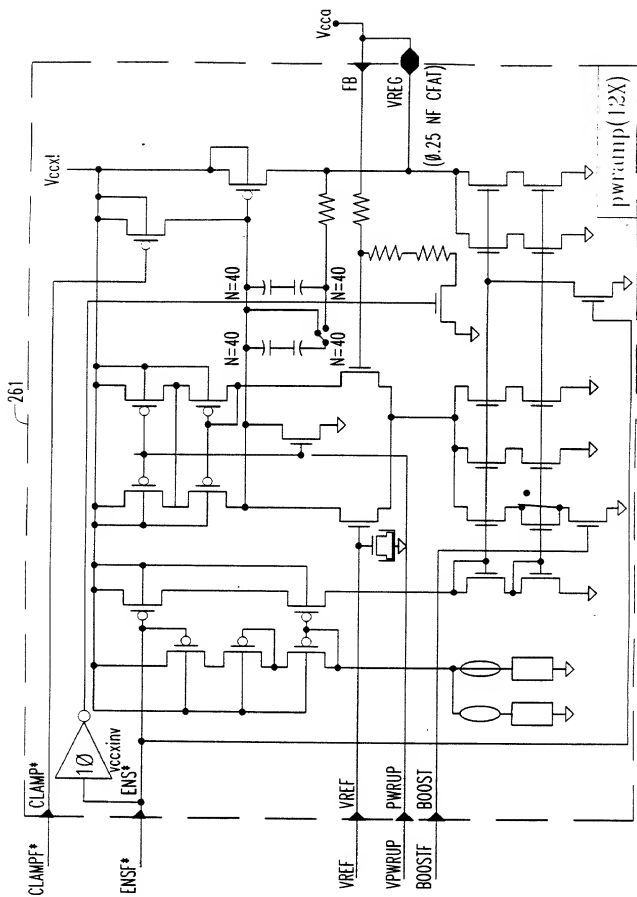
FIG. 36G

DISABLE\*  
(FROM FIG. 36E)

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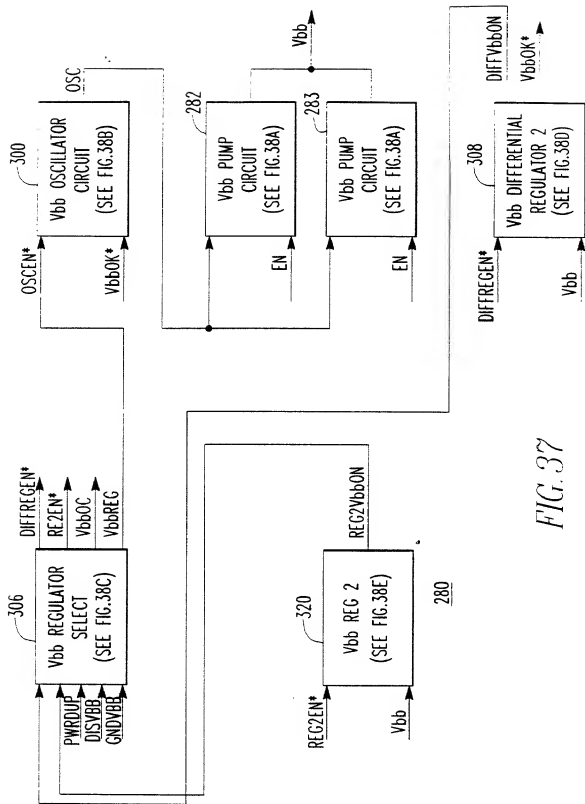


FIG. 37

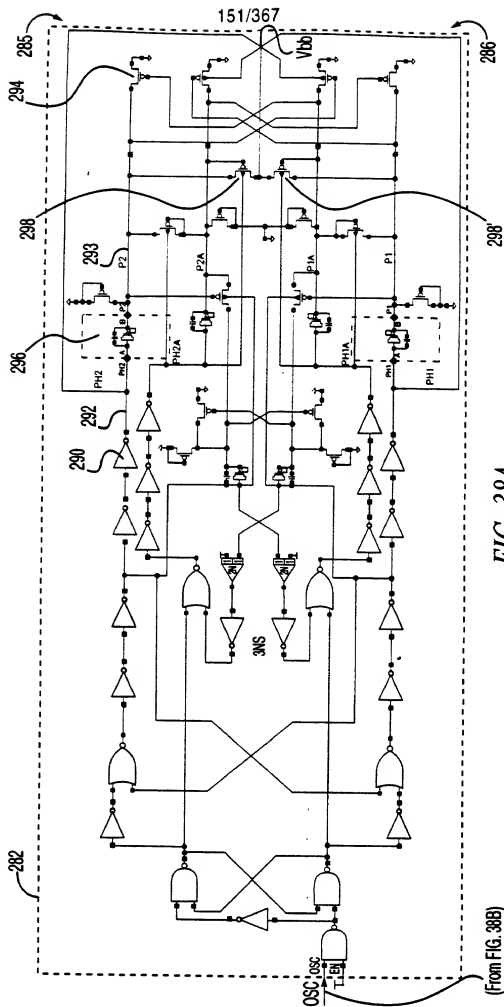
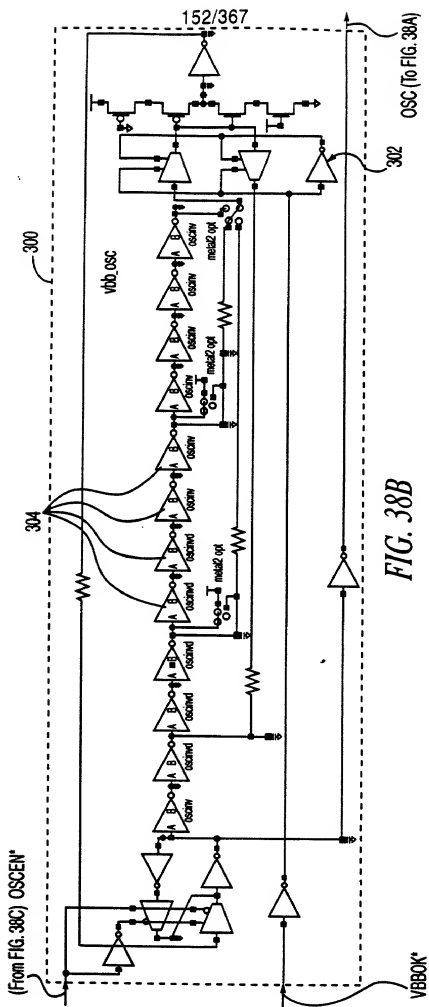


FIG. 38A

(From FIG. 38B)



**FIG. 38B**

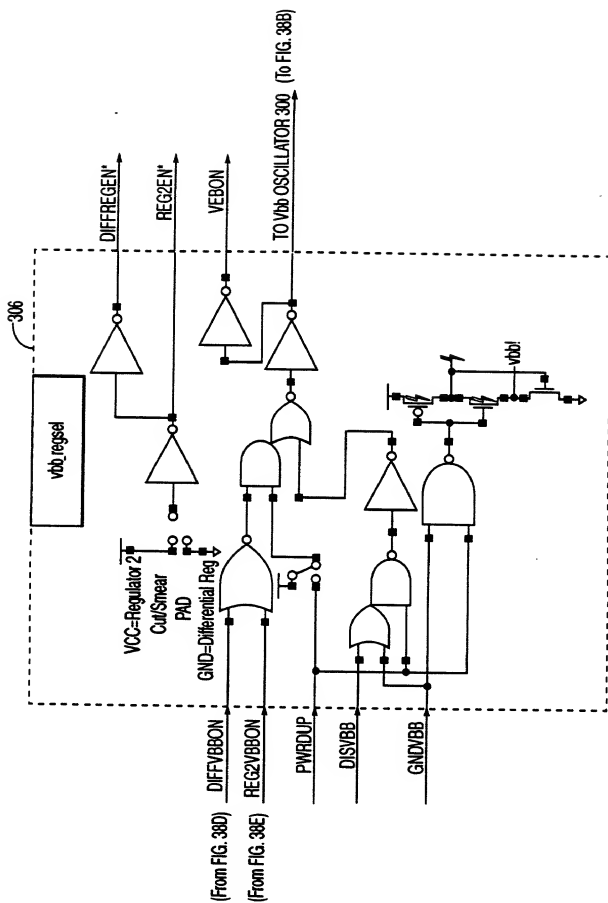


FIG. 38C

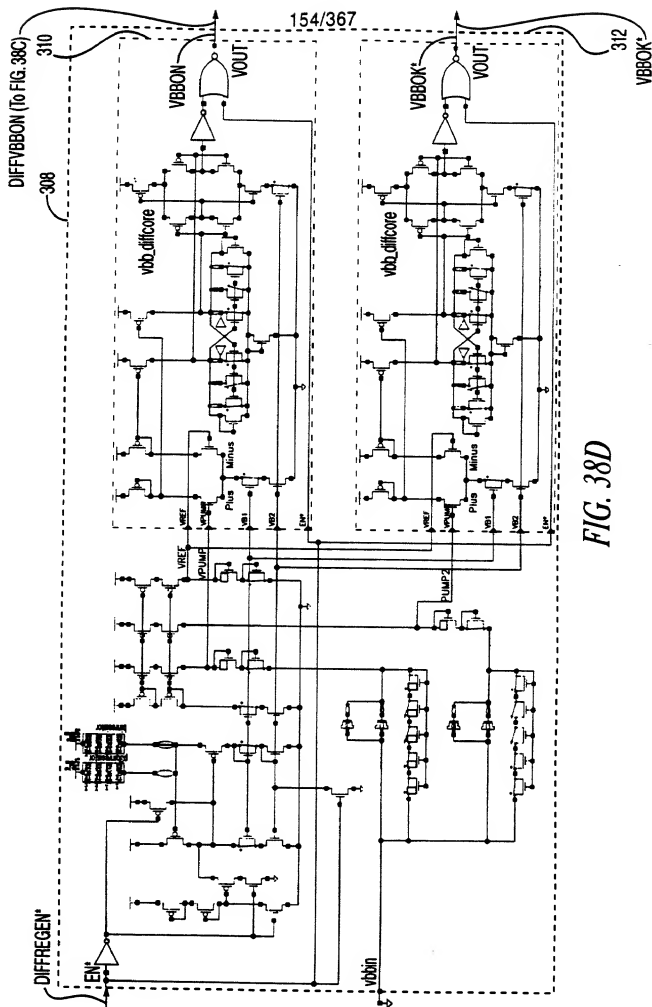
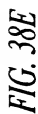


FIG. 38D



**FIG. 38E**

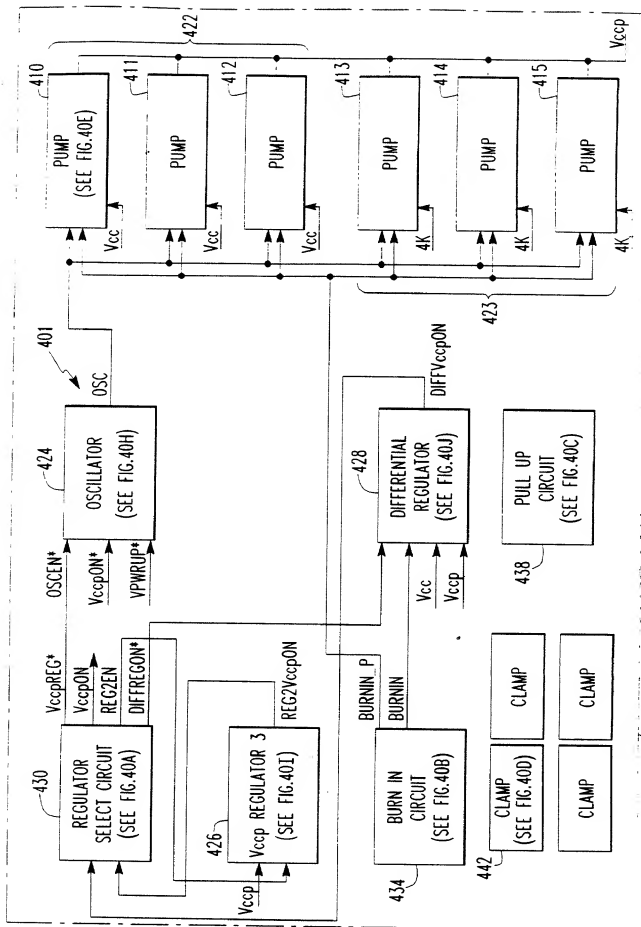


FIG. 39





FIG. 40A

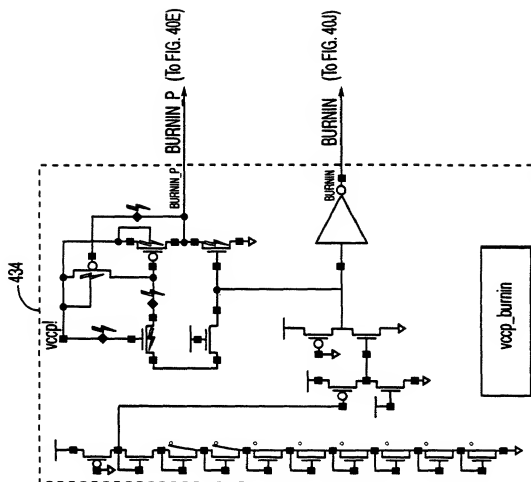
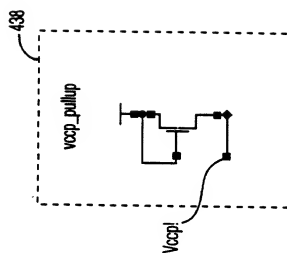


FIG. 40B

*FIG. 40C*

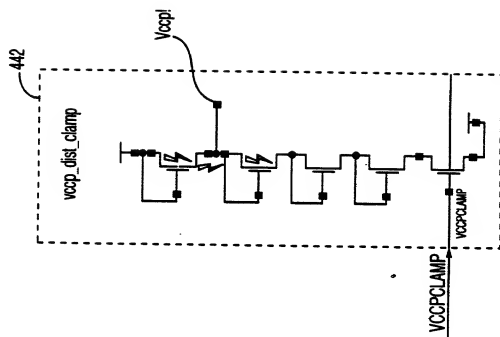
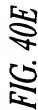


FIG. 40D



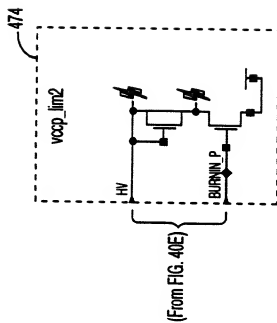


FIG. 40F

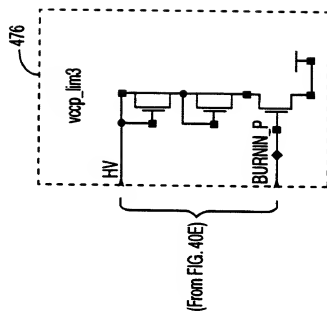
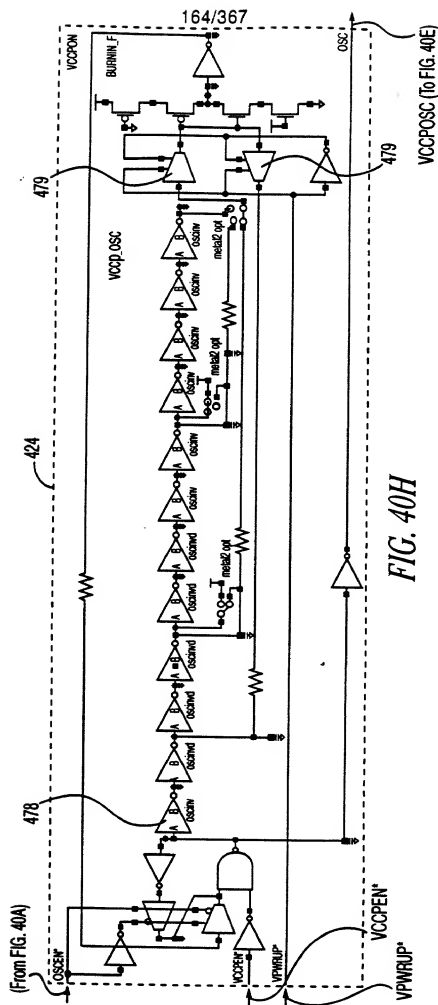


FIG. 40G





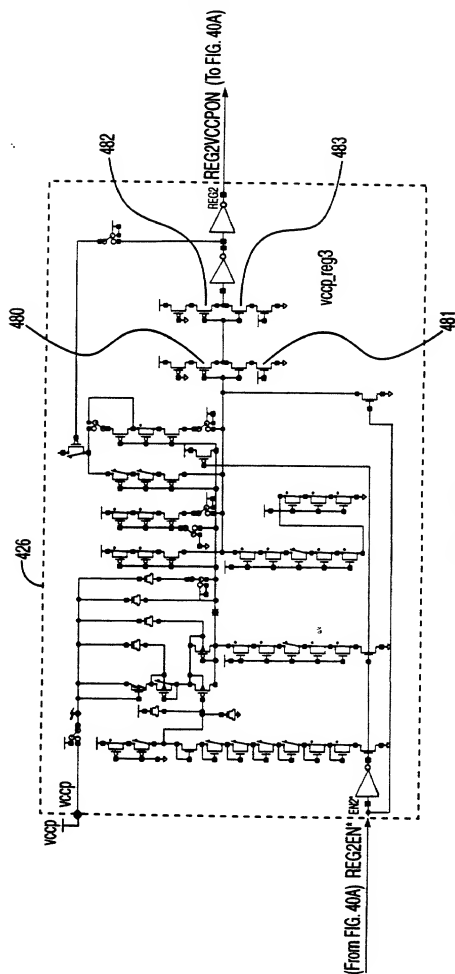
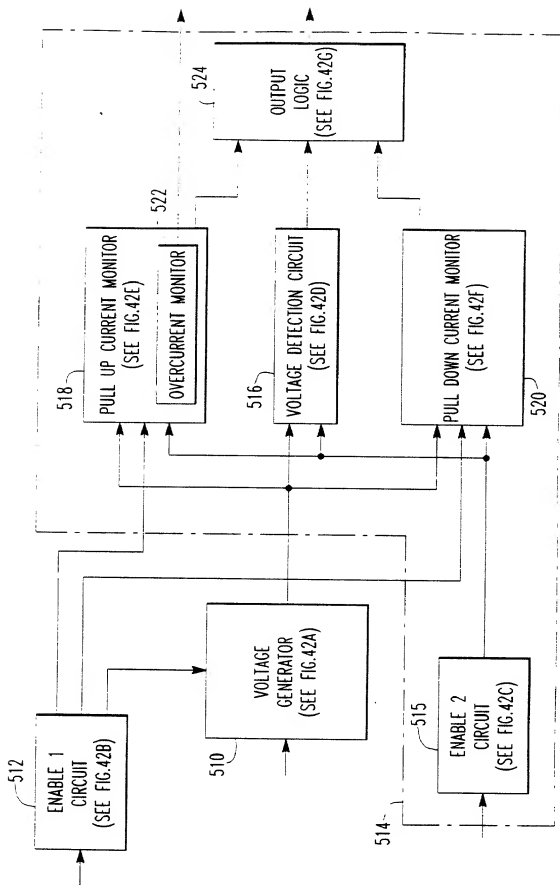


FIG. 40I



FIG. 40J



500

FIG. 11

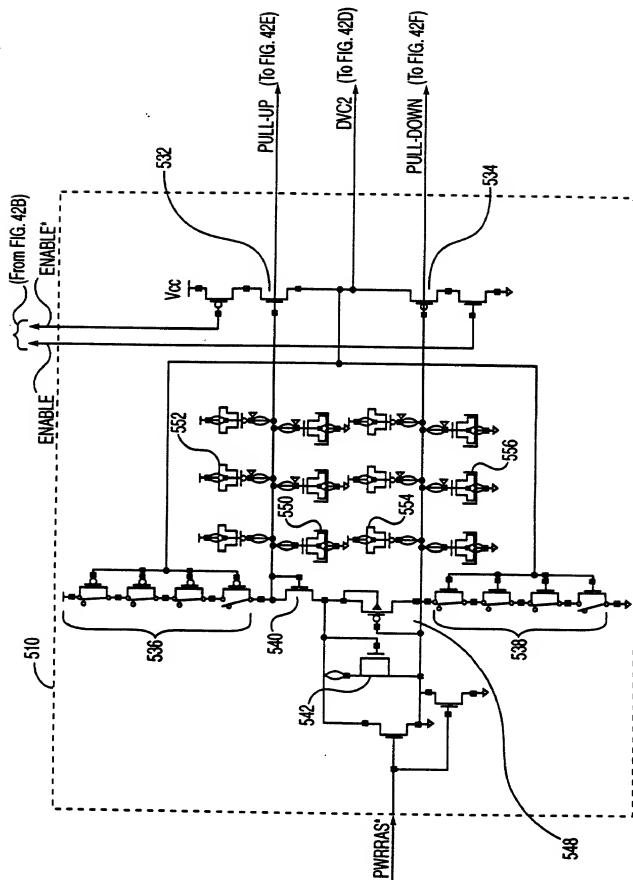


FIG. 42A

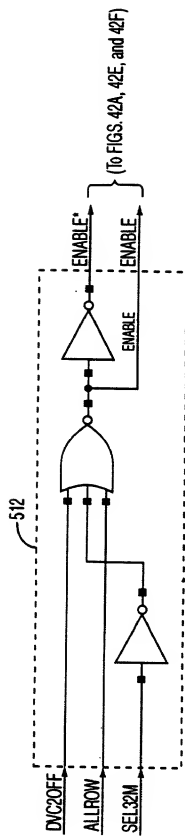


FIG. 42B

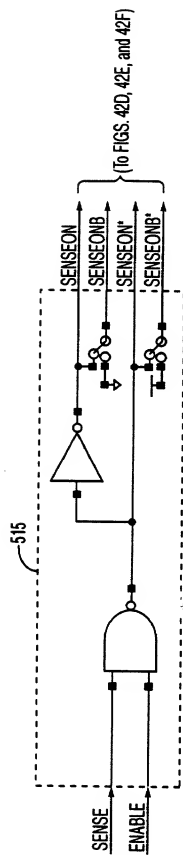


FIG. 42C

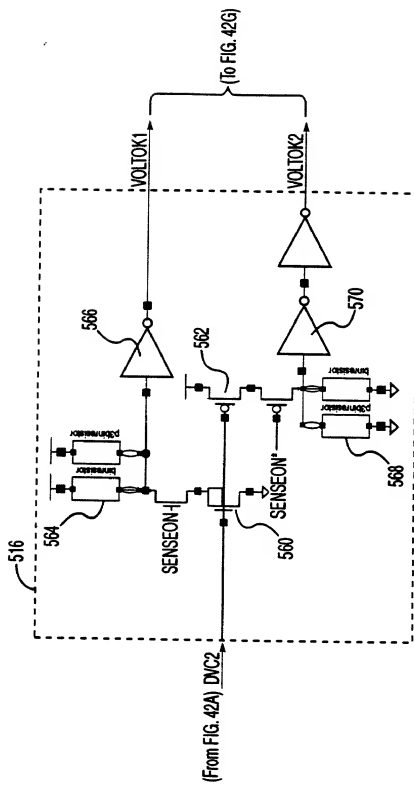


FIG. 42D

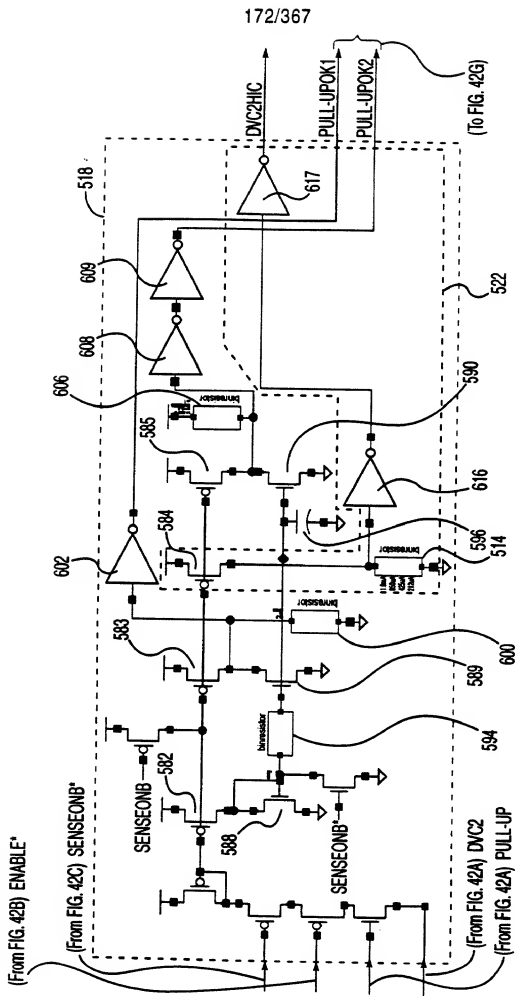


FIG. 42E



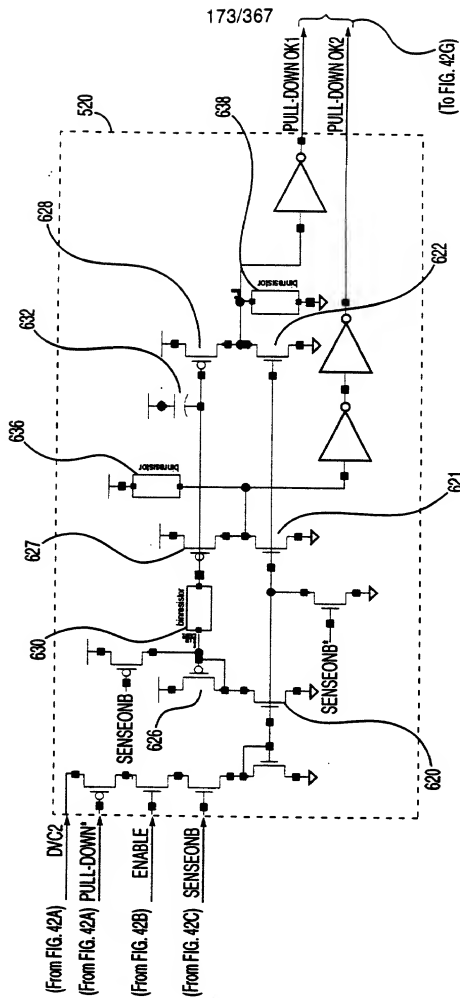


FIG. 42F

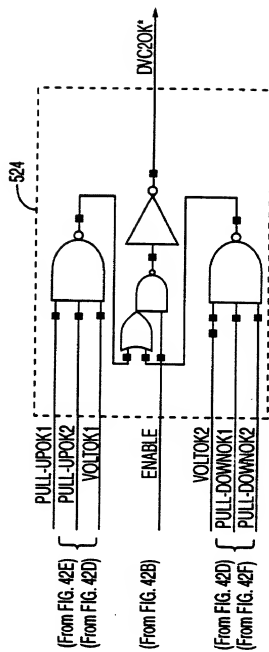


FIG. 42G

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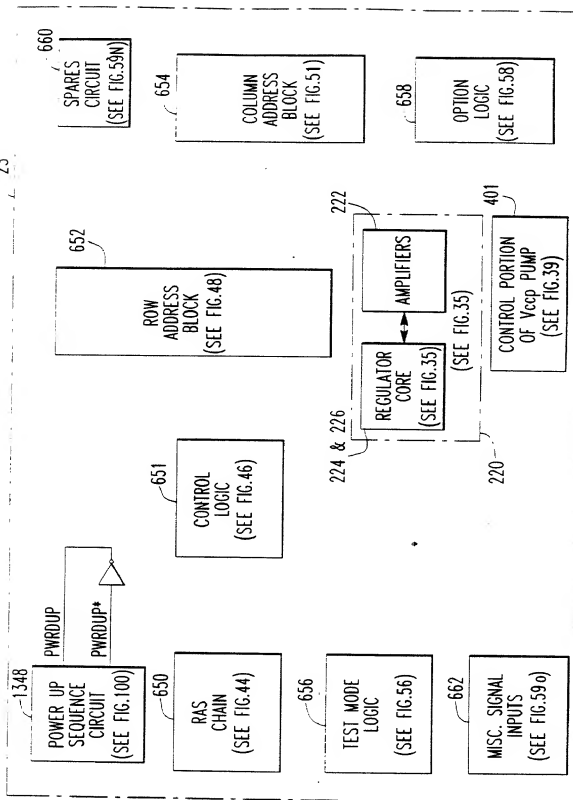


FIG. 43

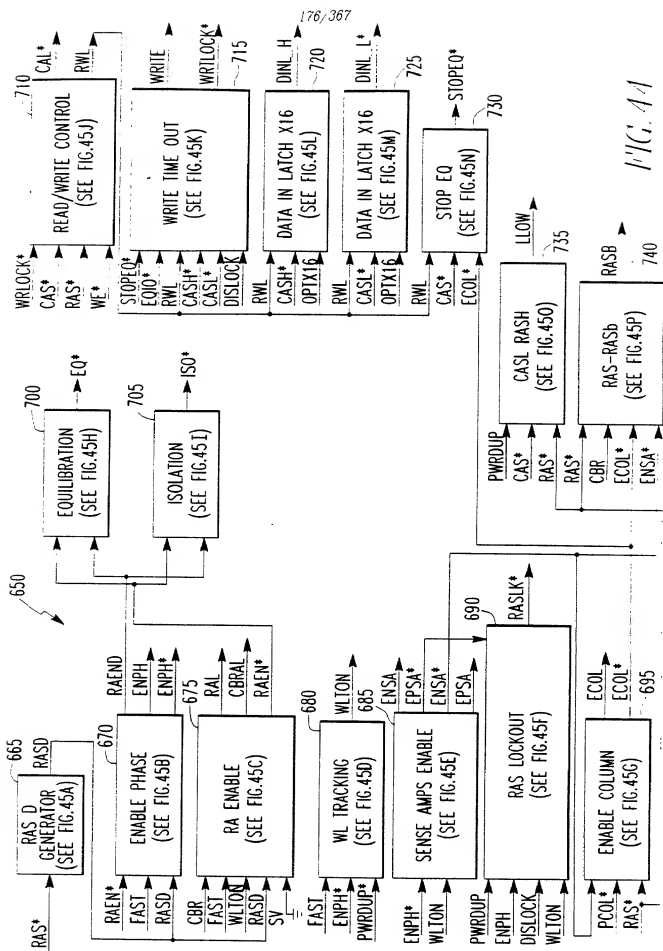


FIG. 41

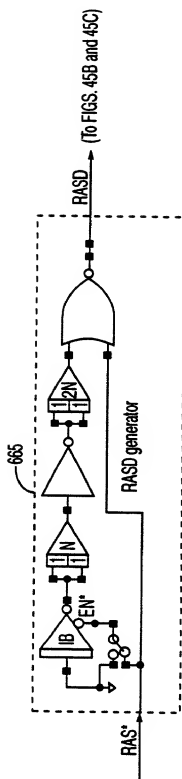


FIG. 45A

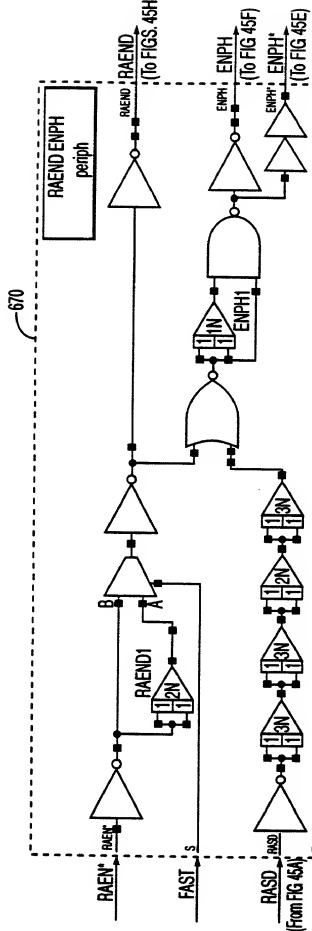


FIG. 45B

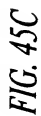
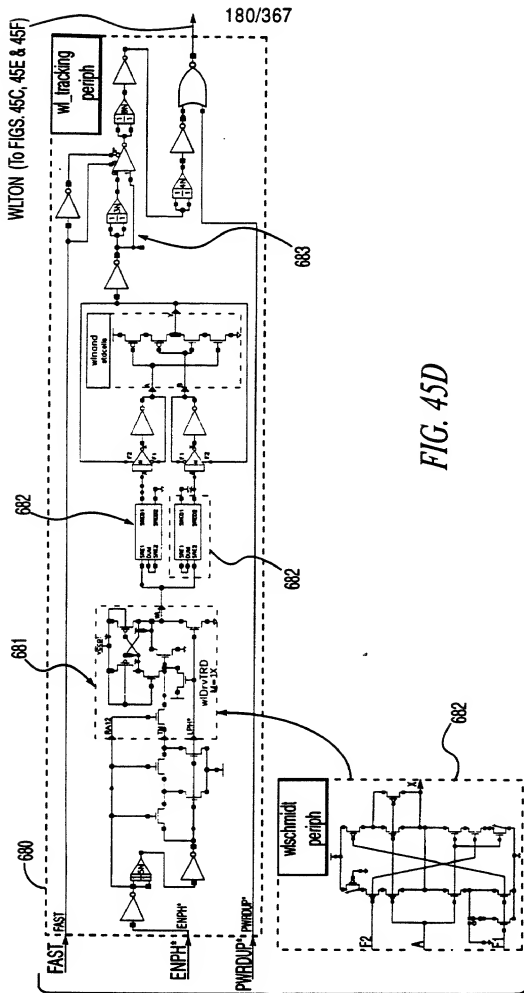


FIG. 45C



(From FIG. 45B)



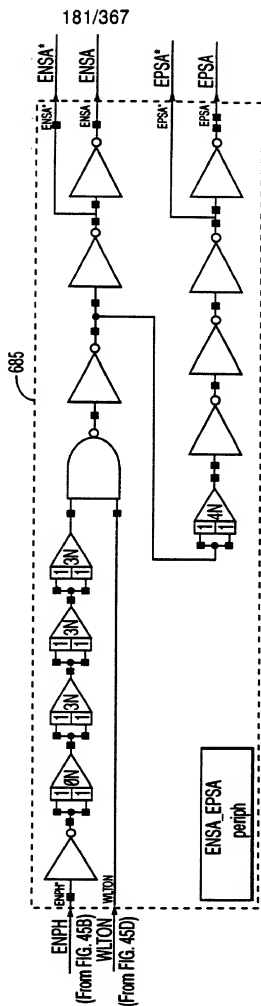


FIG. 45E

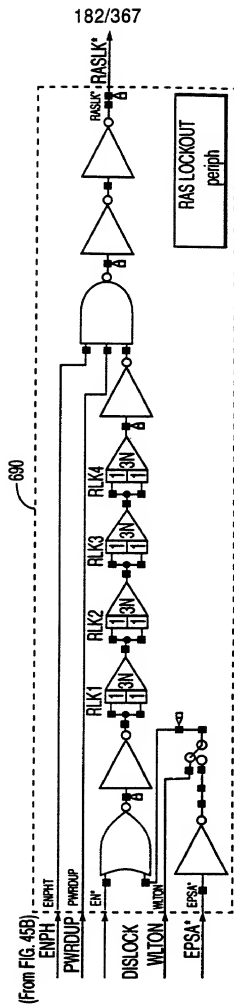


FIG. 45F

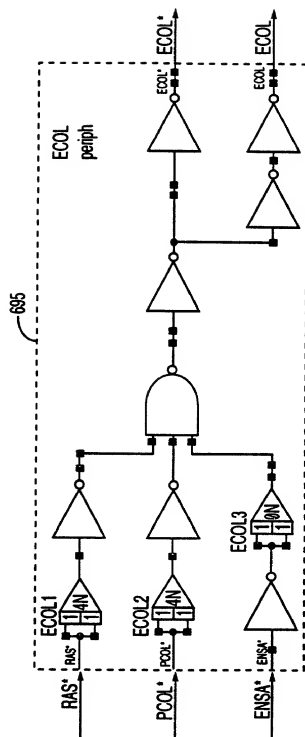


FIG. 45G

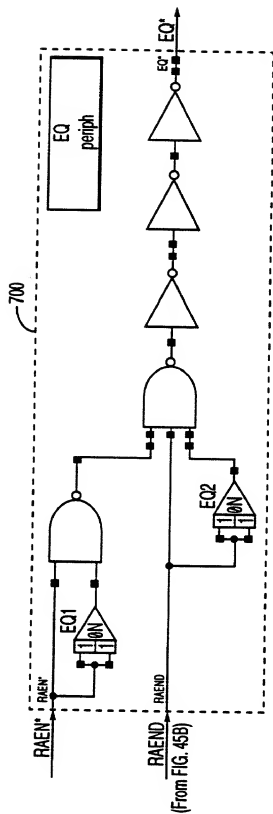


FIG. 45H

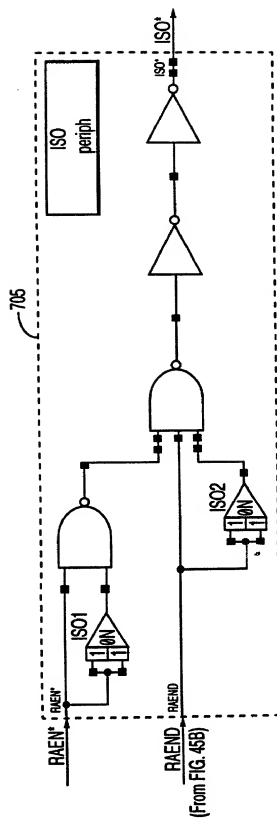
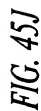


FIG. 45I



**FIG. 45J**

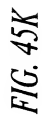


FIG. 45K



FIG. 45L





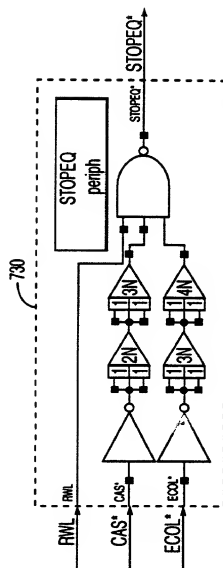


FIG. 45N

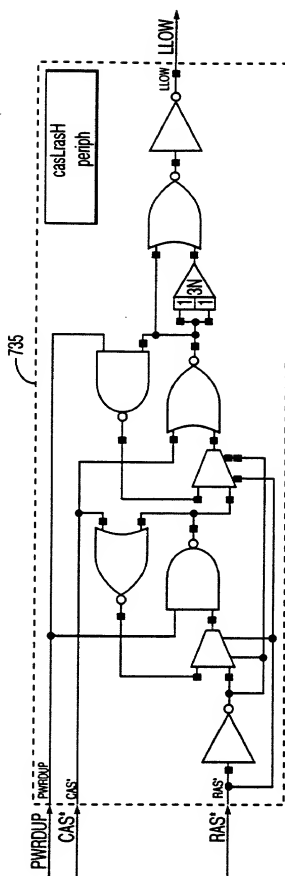


FIG. 450

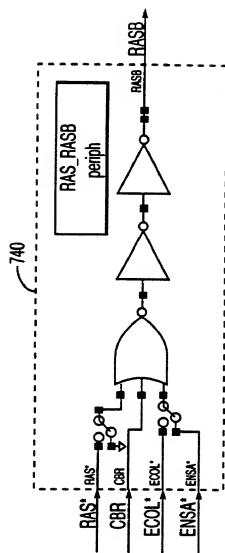
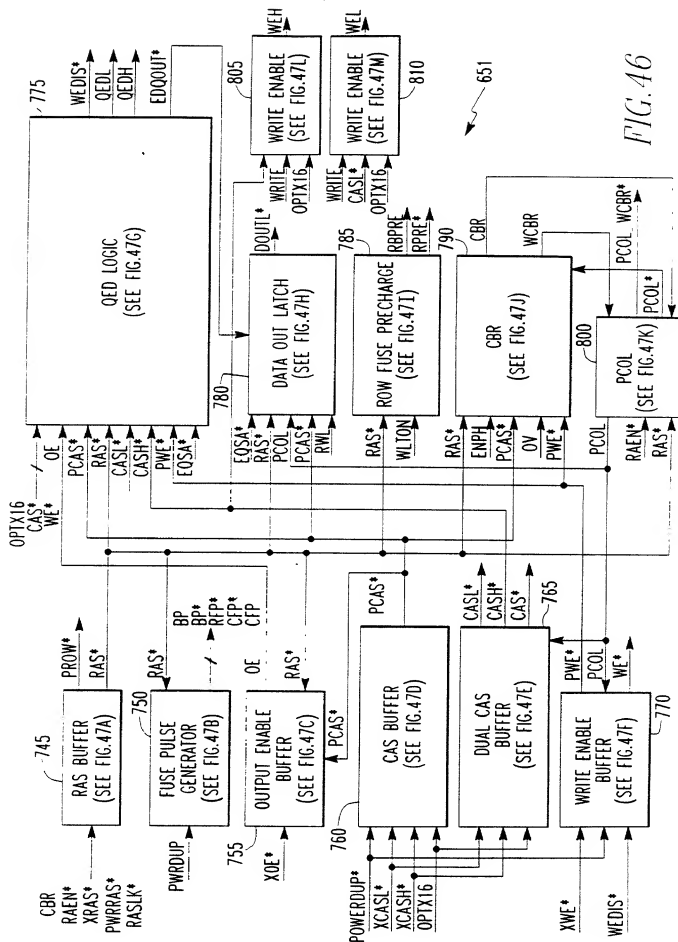


FIG. 45P



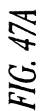


FIG. 47A

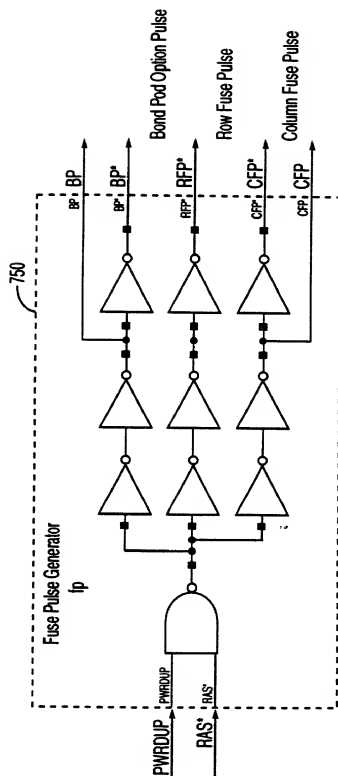


FIG. 47B

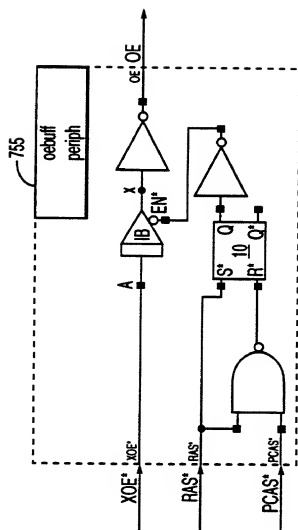


FIG. 47C



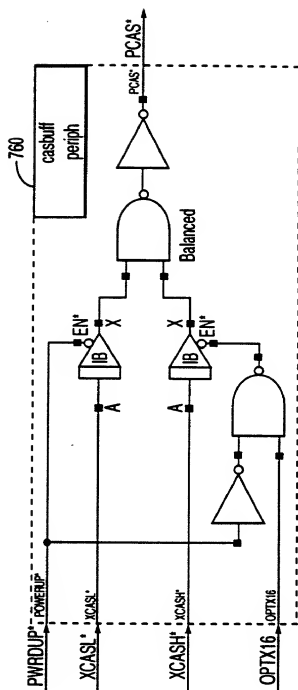


FIG. 47D

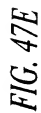


FIG. 47E

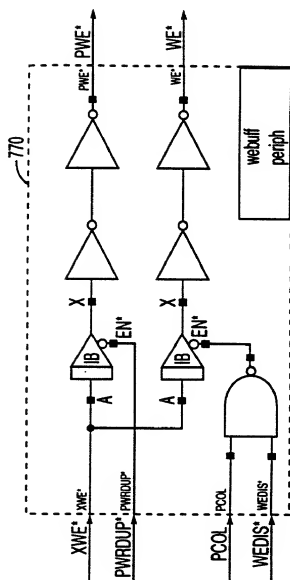


FIG. 47F

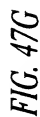


FIG. 47G

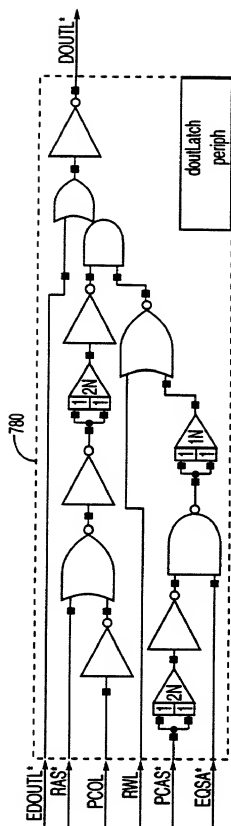
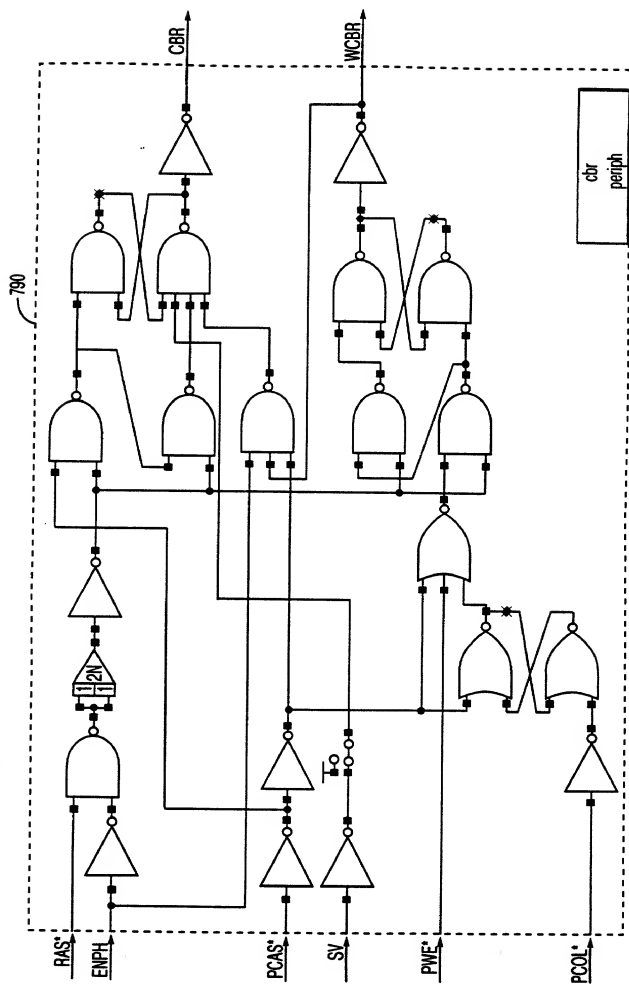


FIG. 47H





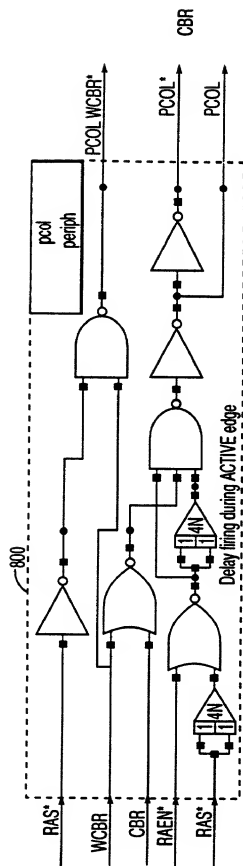


FIG. 47K



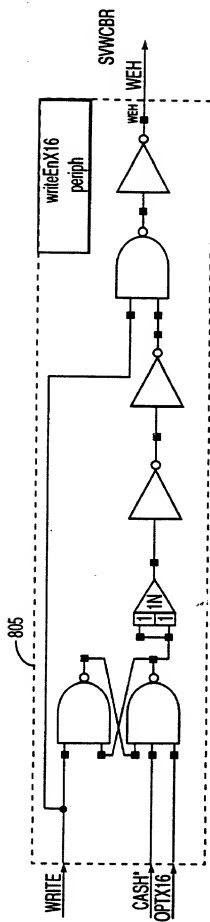


FIG. 47L

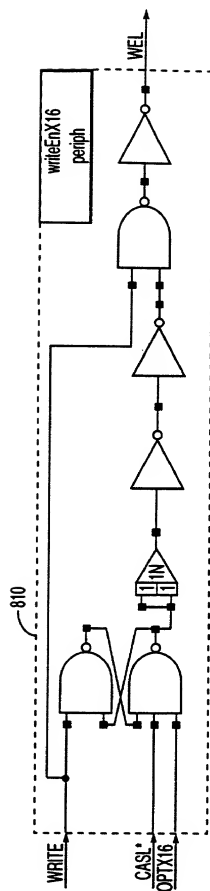


FIG. 47M



FIG. 48A

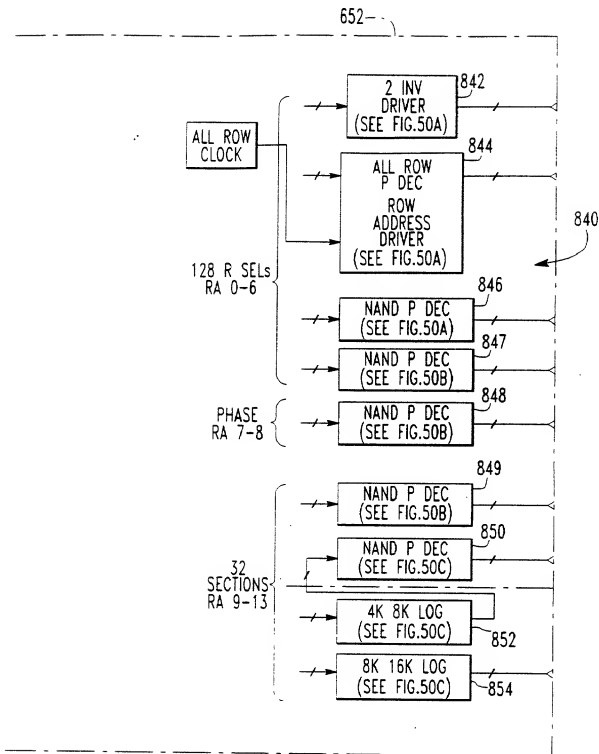


FIG. 48B

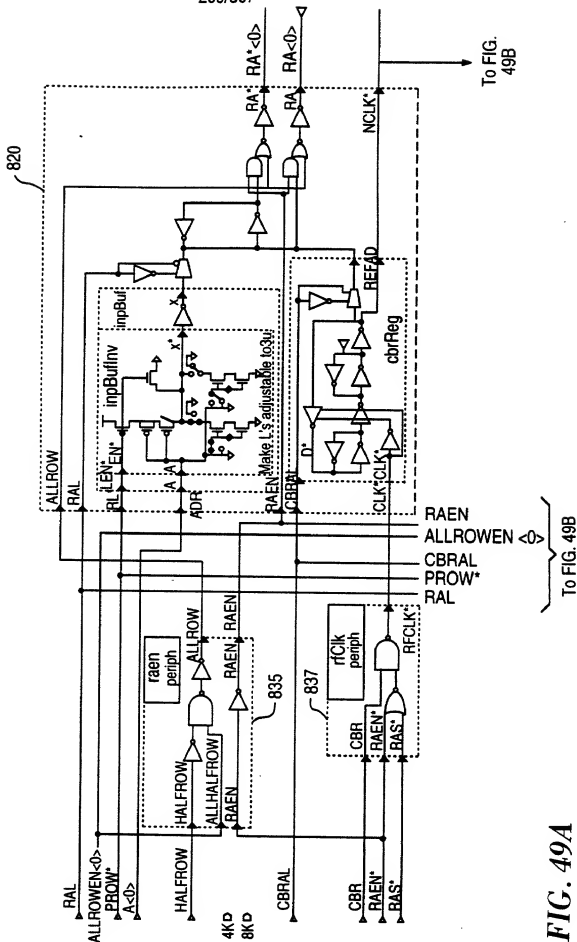
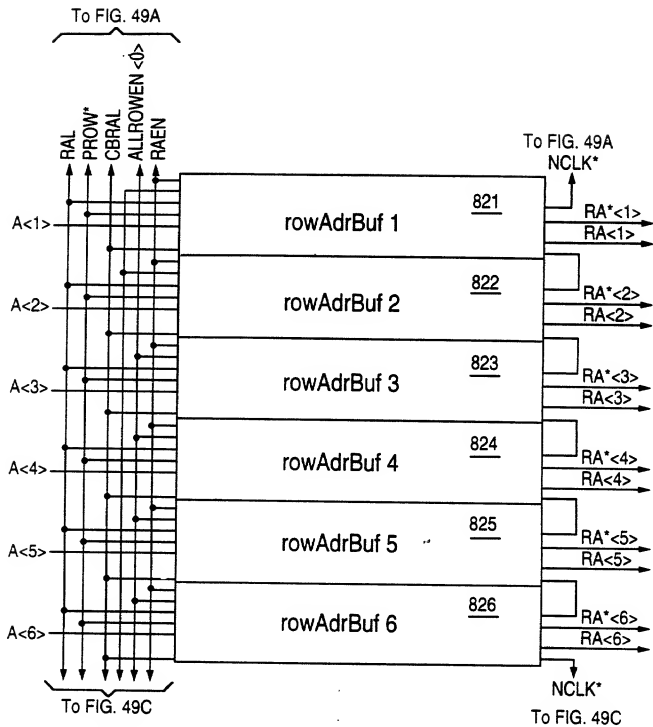


FIG. 49A

**FIG. 49B**

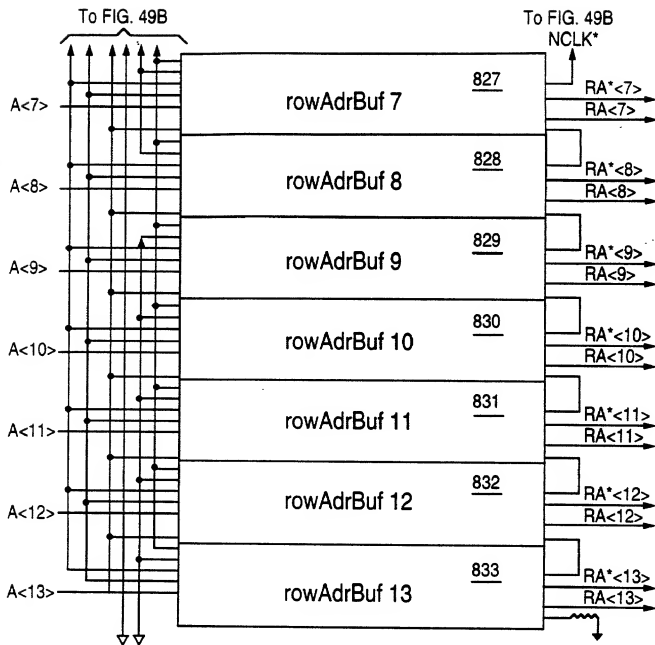


FIG. 49C

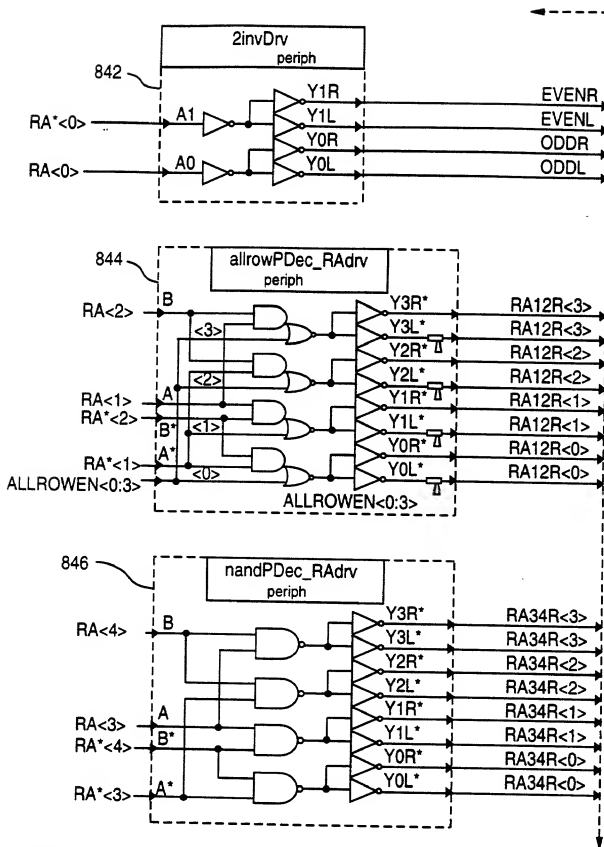
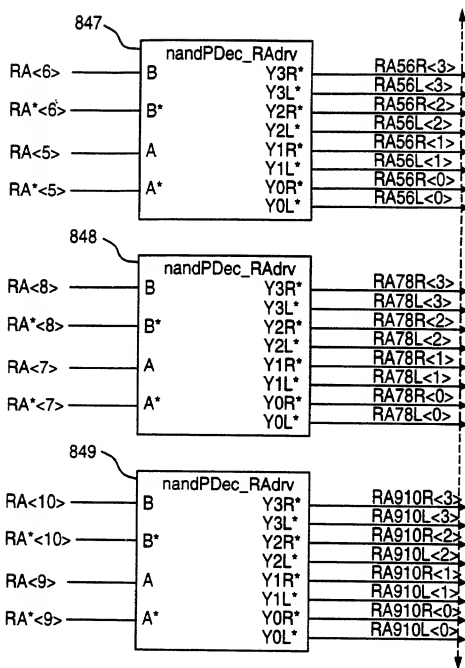


FIG. 50A



**FIG. 50B**

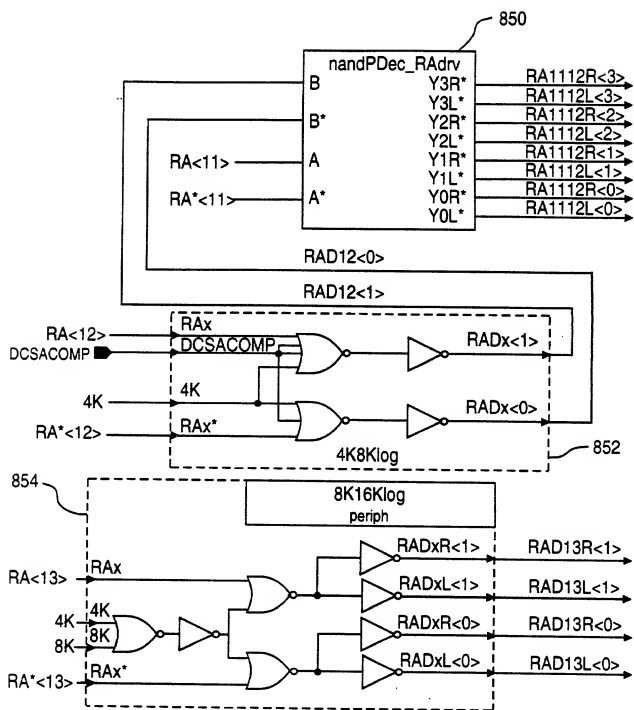


FIG. 50C

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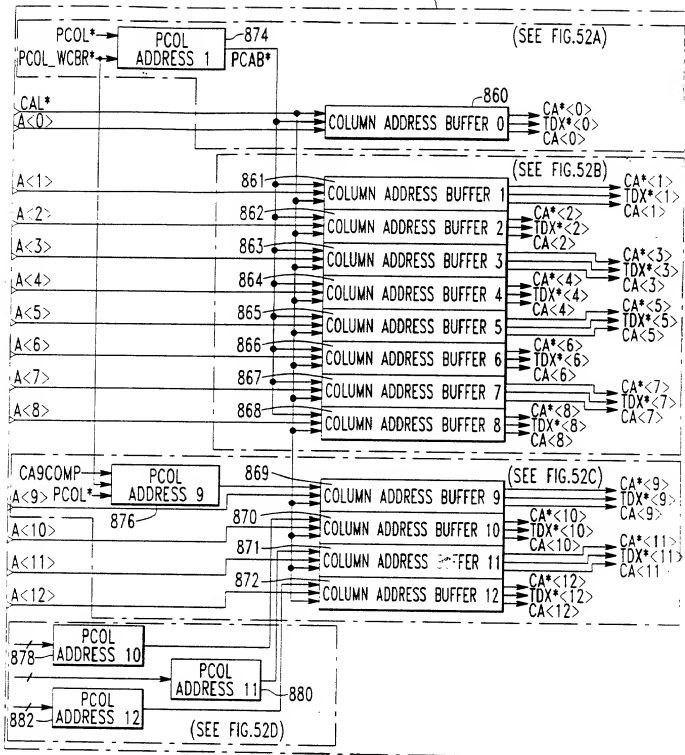


FIG. 51A

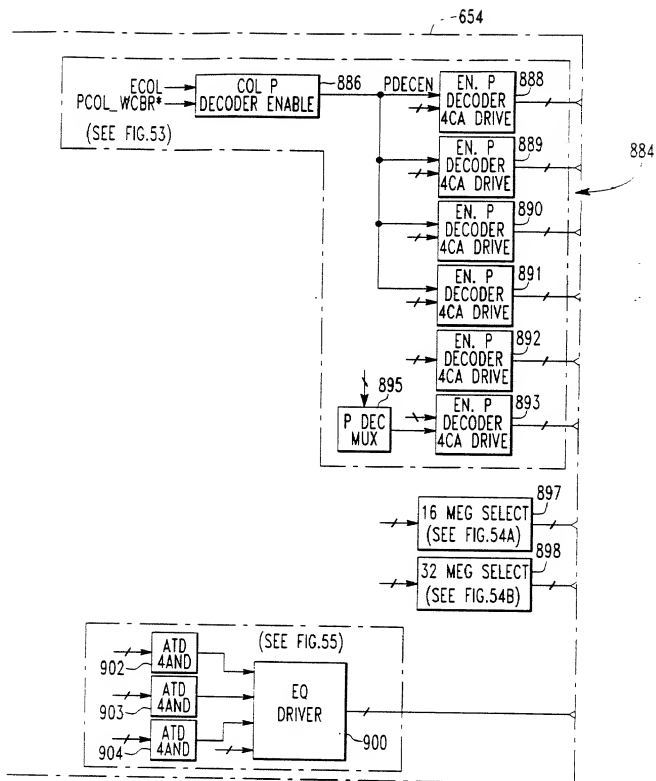


FIG. 51B



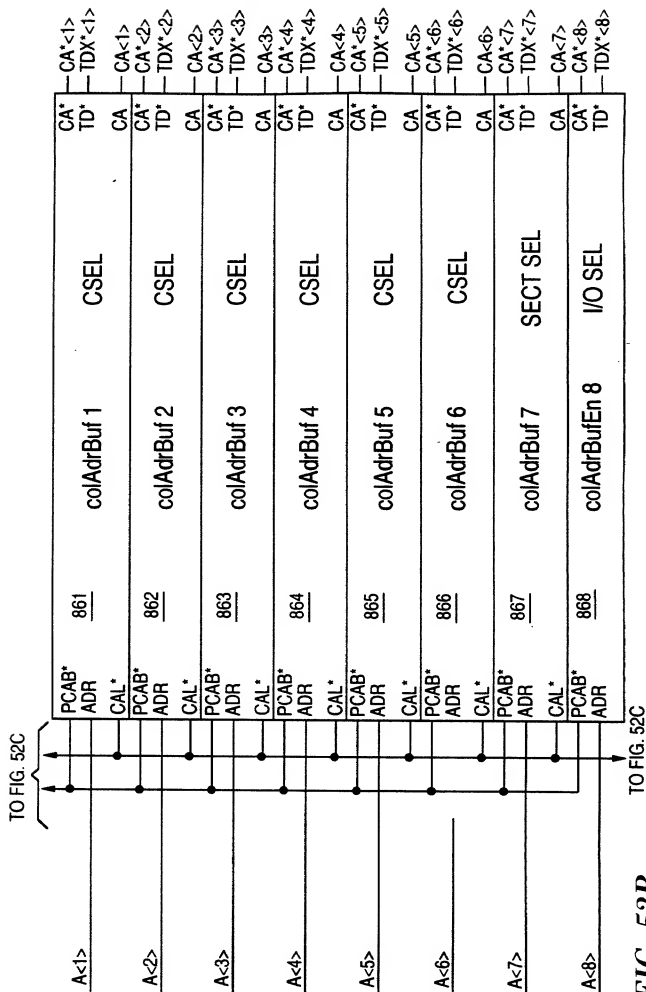
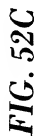


FIG. 52B



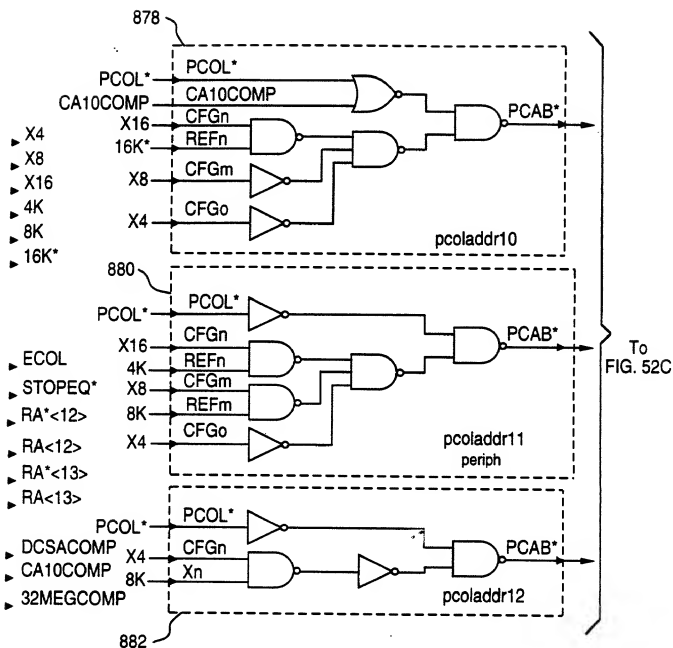
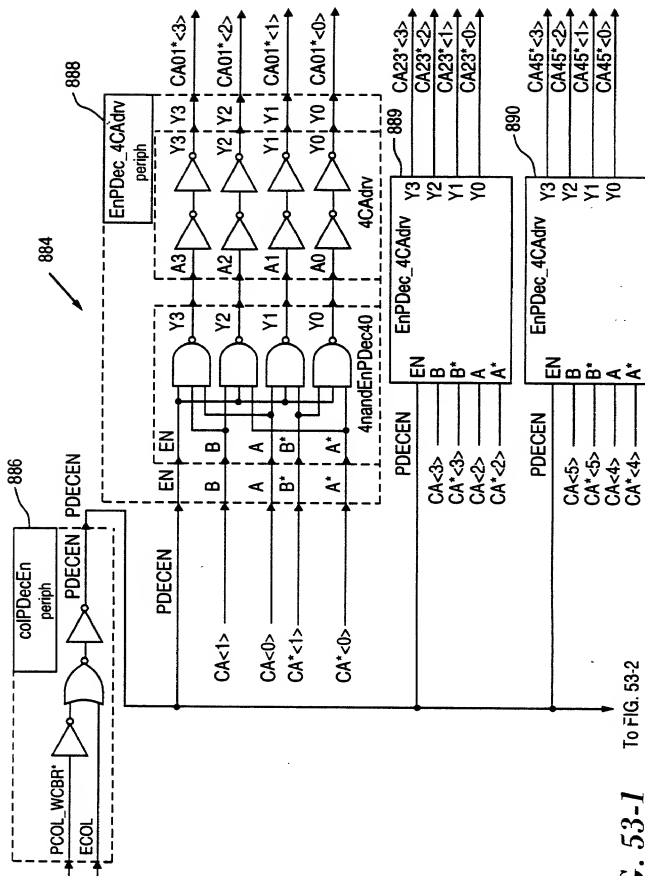


FIG. 52D





To FIG. 53.2

FIG. 53-1

To FIG. 53-1

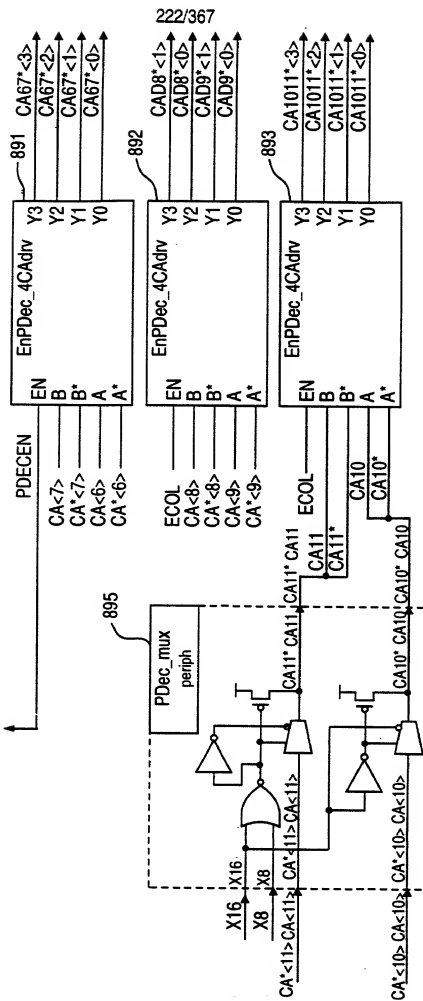


FIG. 53-2

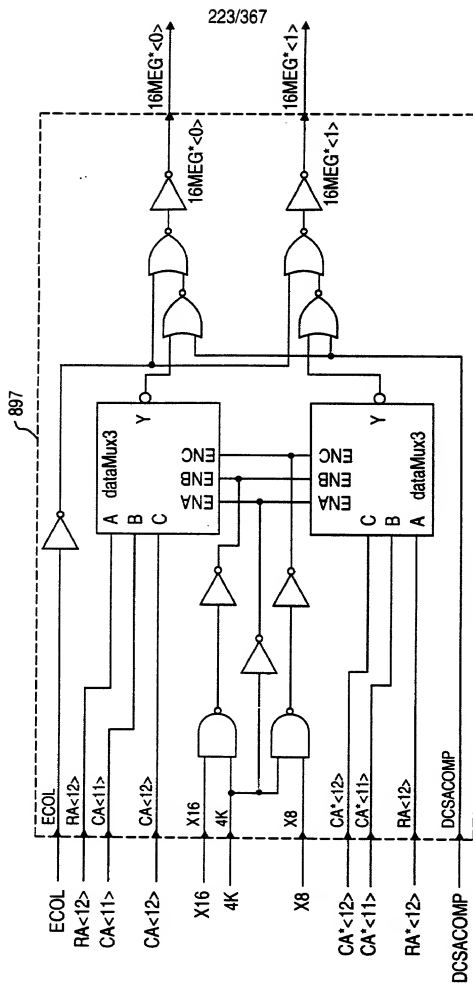


FIG. 54A

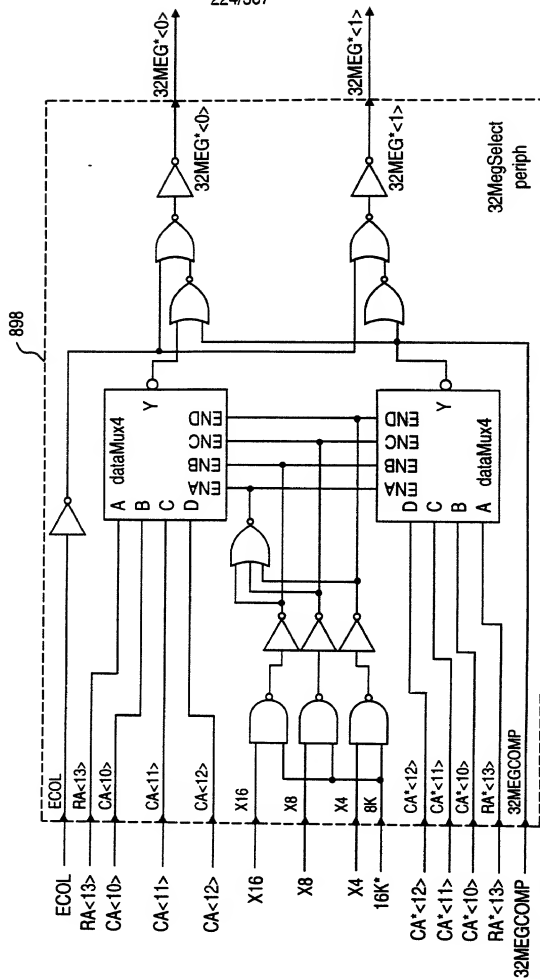
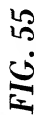


FIG. 54B



**FIG. 55**

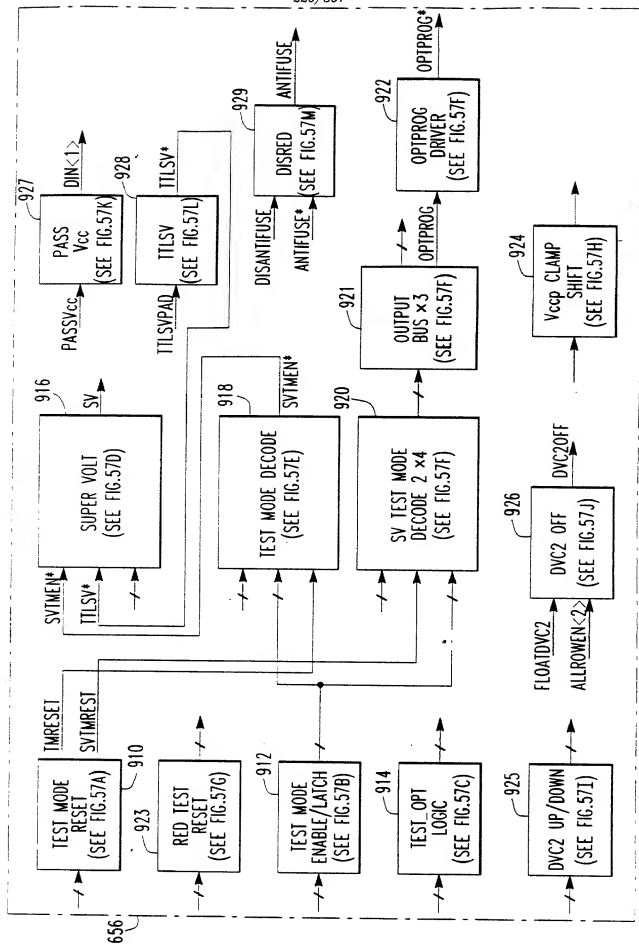


FIG. 56

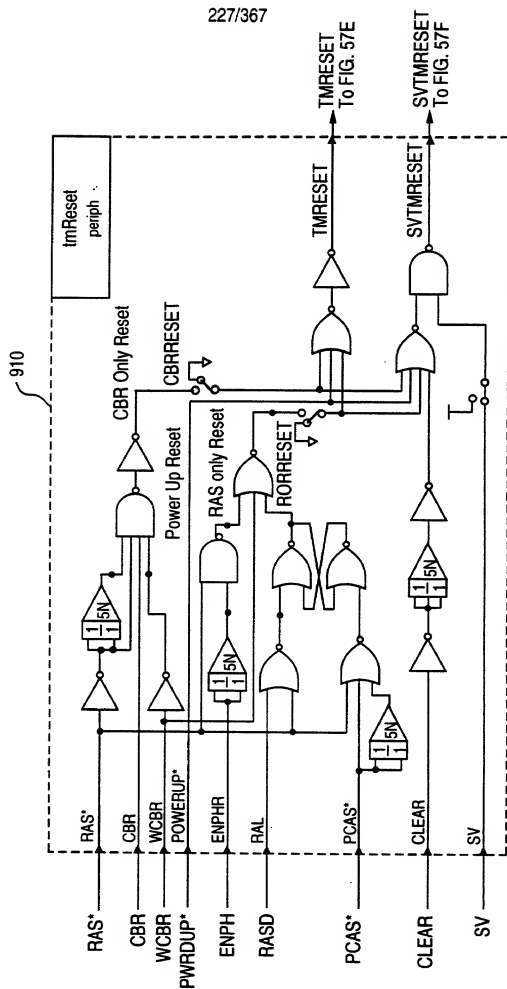


FIG. 57A



**FIG. 57B**



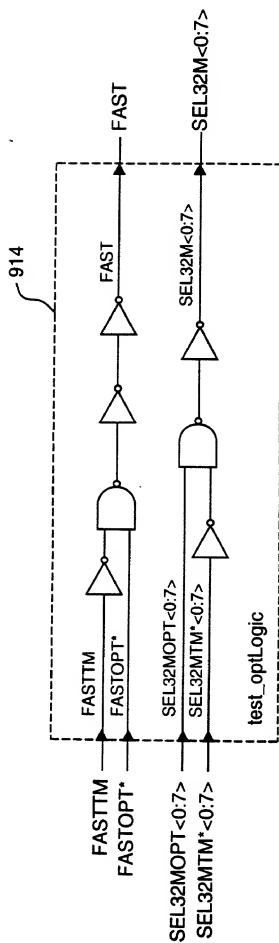
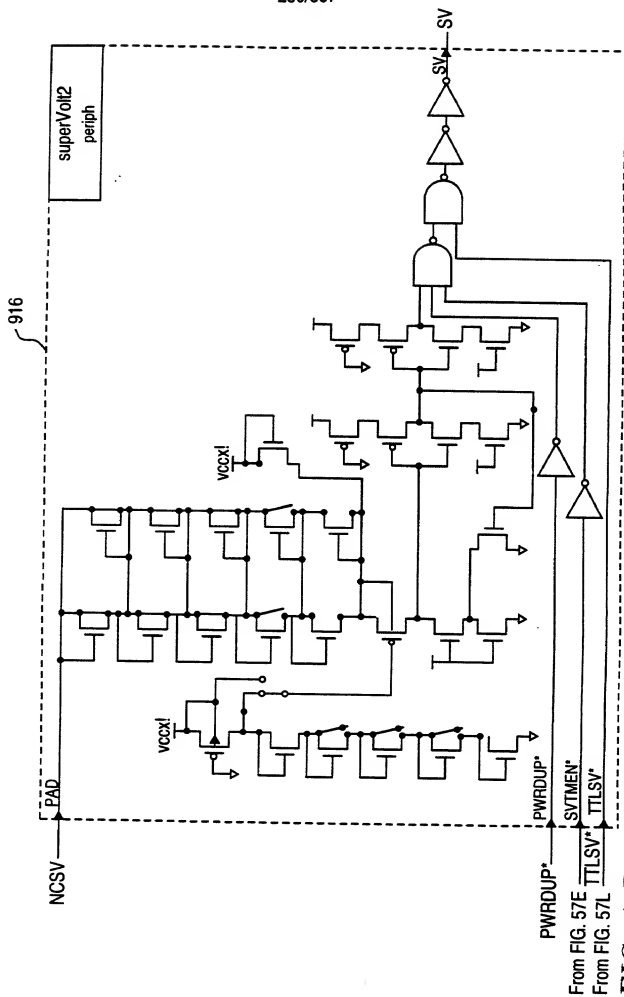
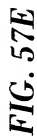
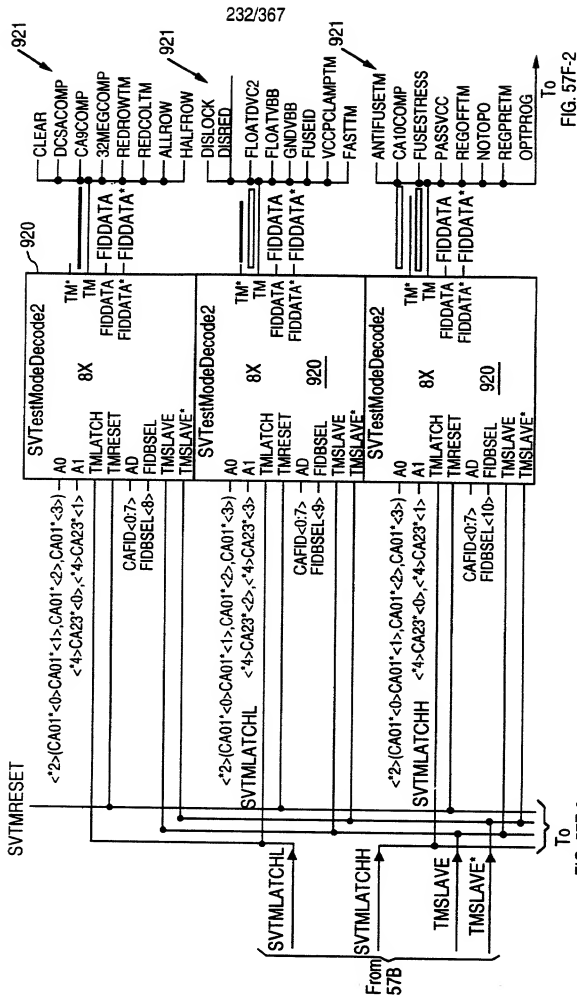


FIG. 57C





**FIG. 57E**



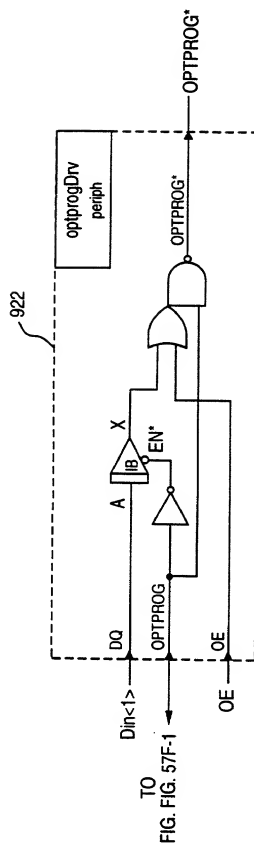


FIG. 57F-2

FIG. 57F-1

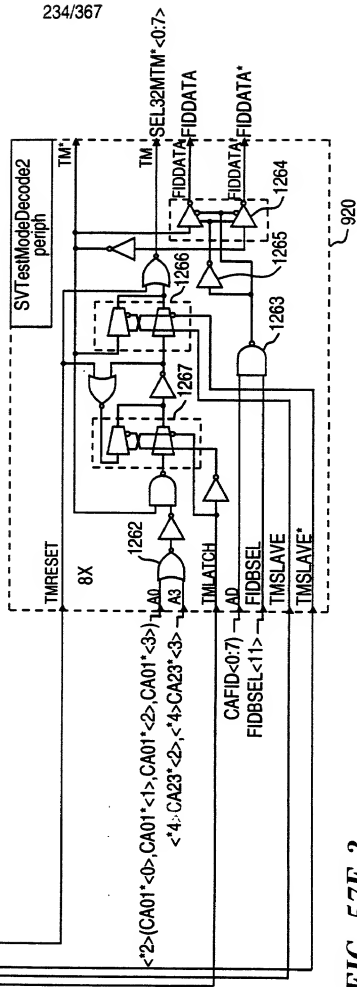


FIG. 57F-3

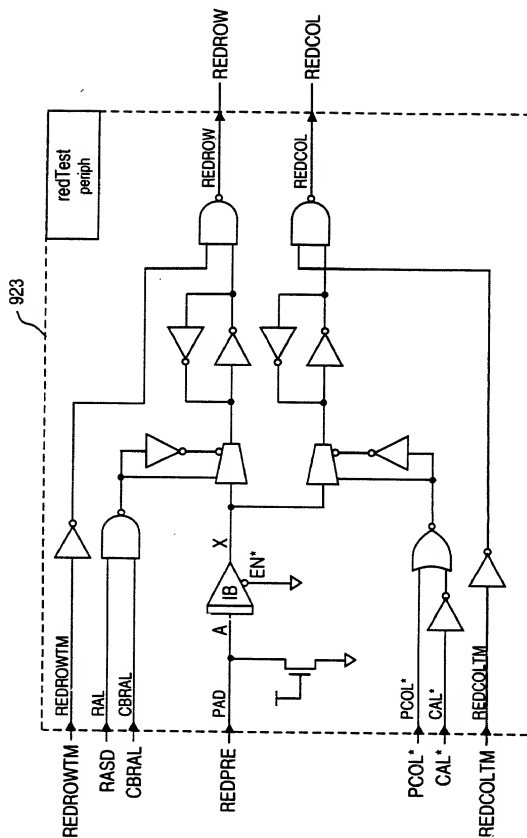
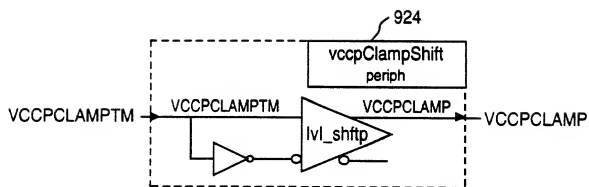
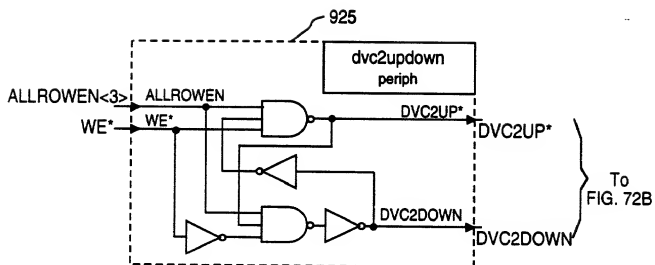
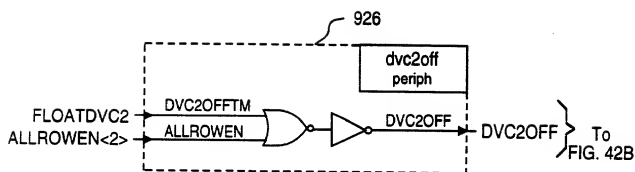


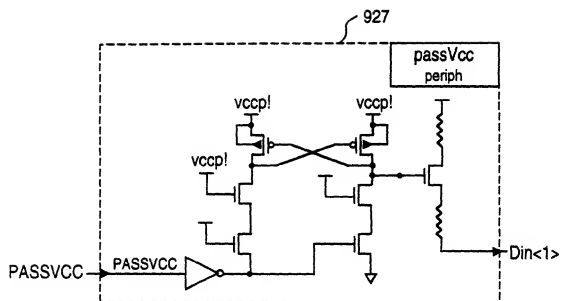
FIG. 57G

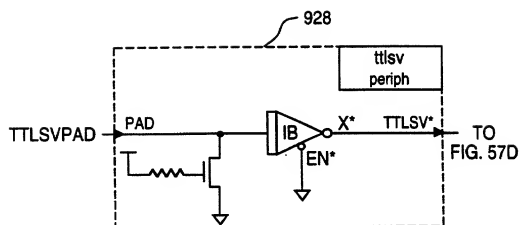
**FIG. 57H**

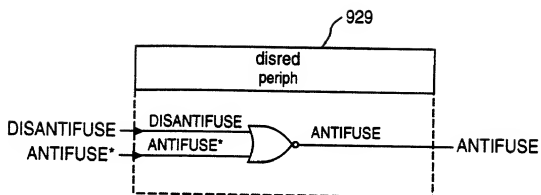


**FIG. 57I**

**FIG. 57J**

**FIG. 57K**

**FIG. 57L**

**FIG. 57M**

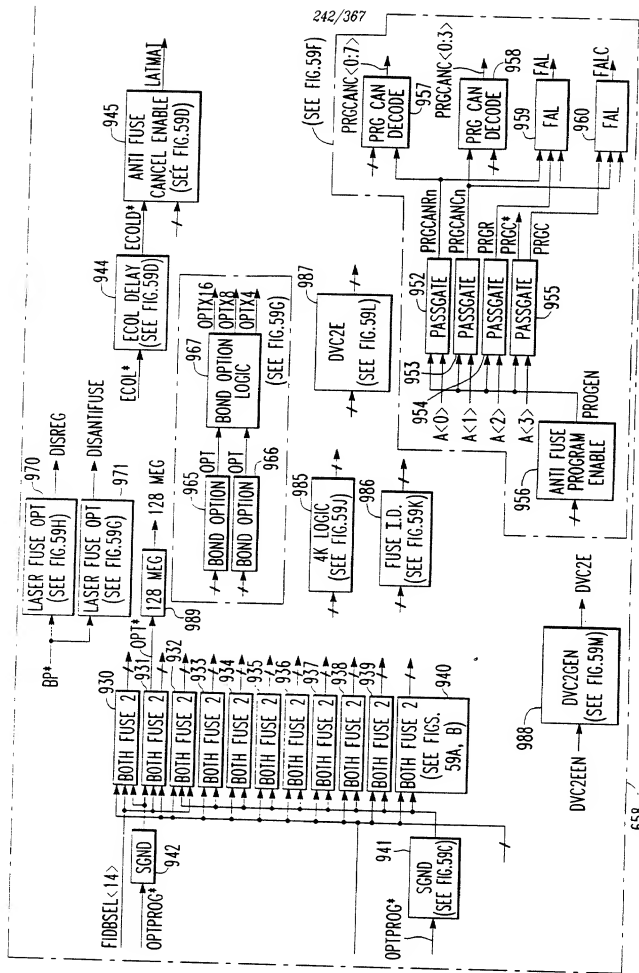


FIG. 58A

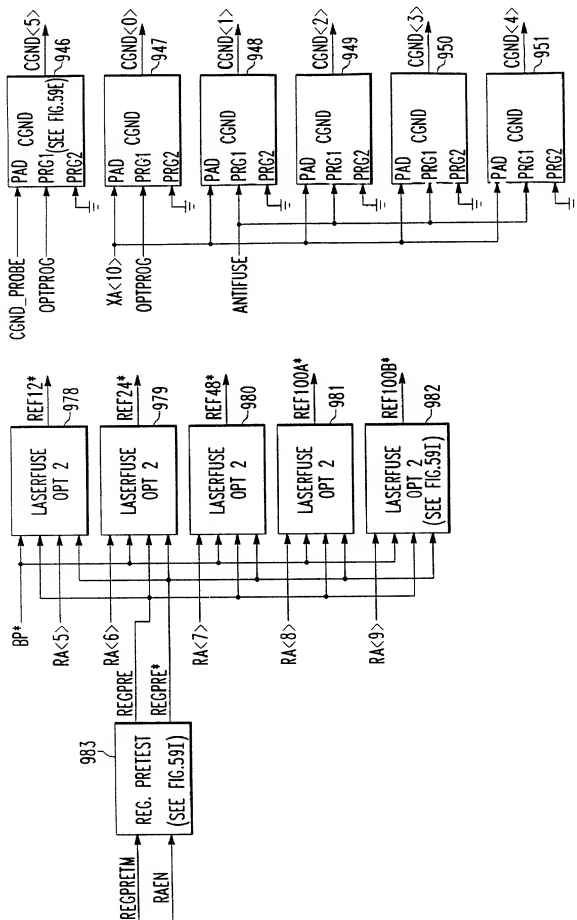


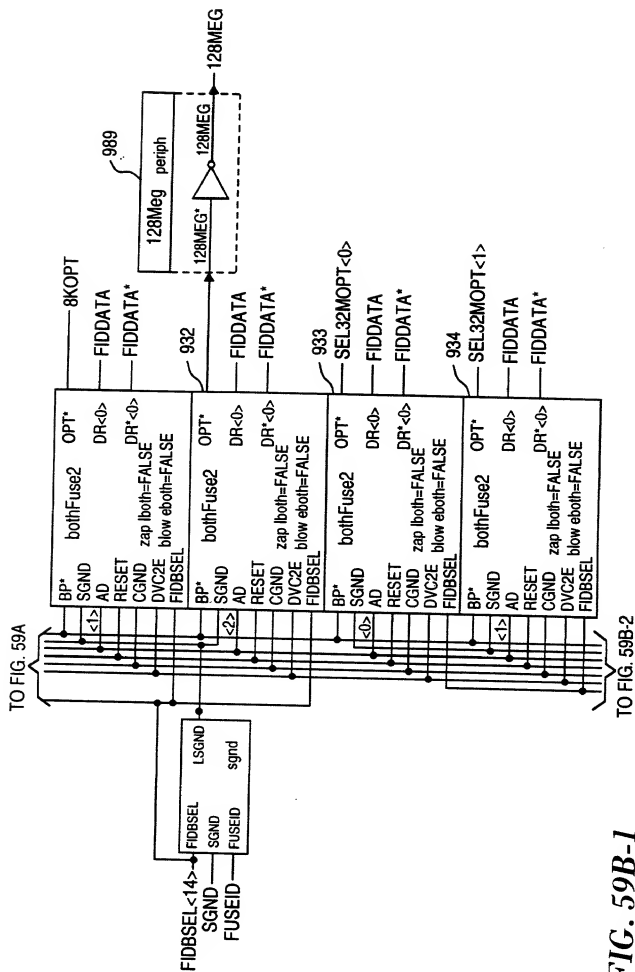
FIG. 58B



FIG. 59B

**FIG. 59A**





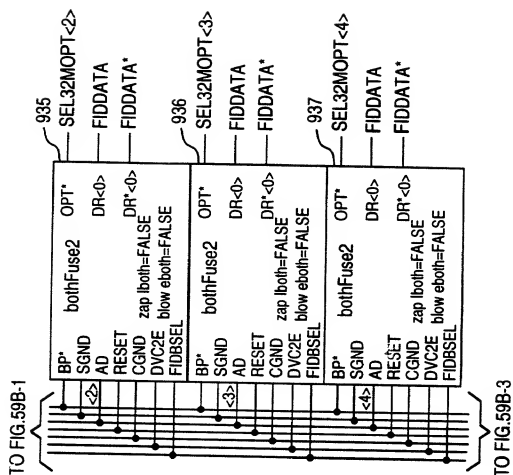


FIG. 59B-2

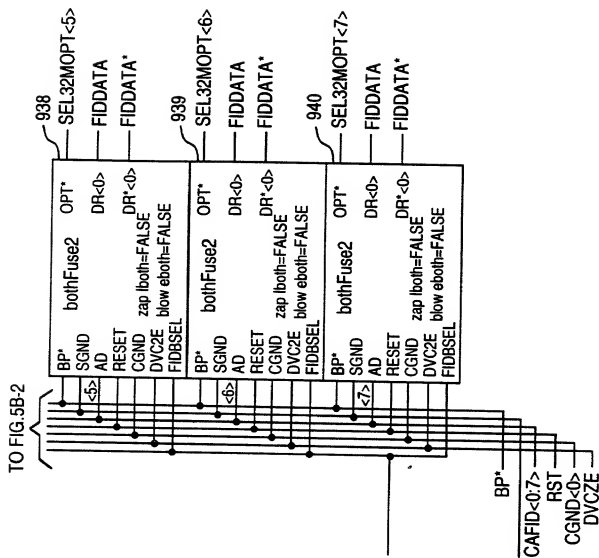
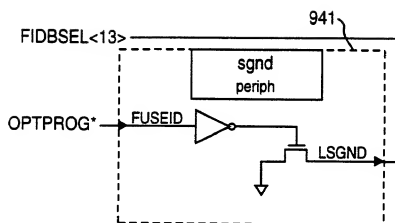
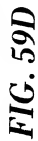


FIG. 59B-3

**FIG. 59C**



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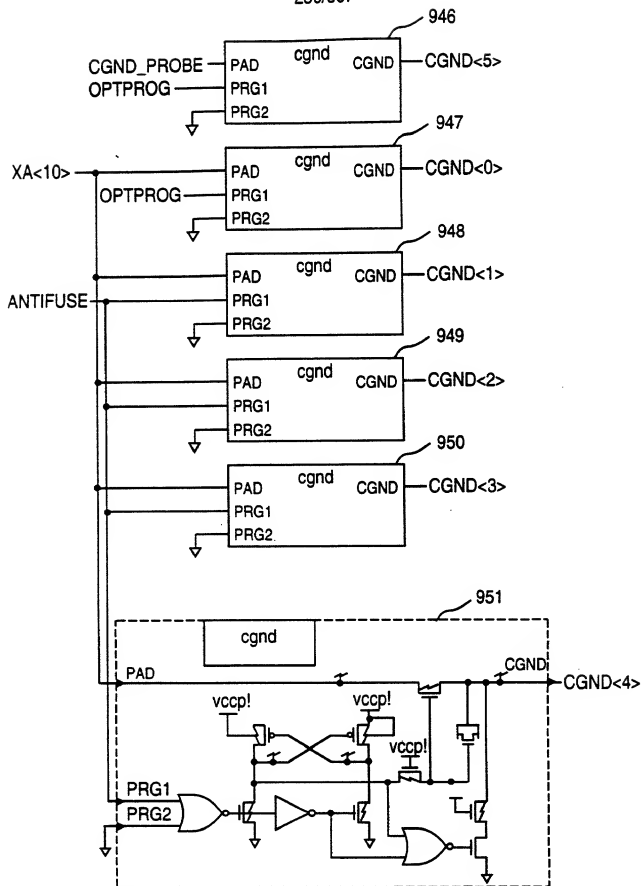
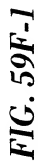
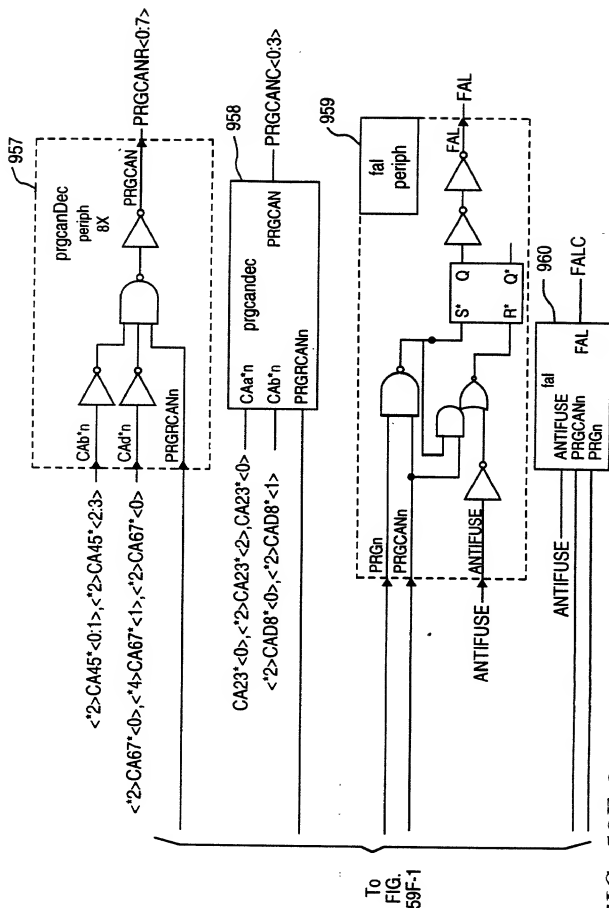


FIG. 59E







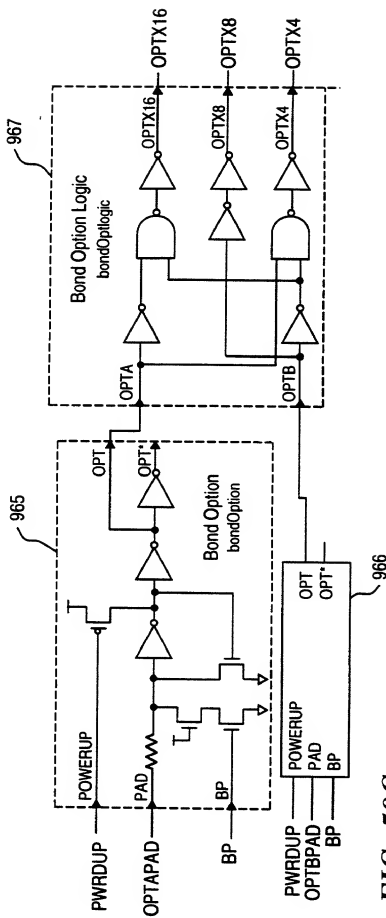


FIG. 59G

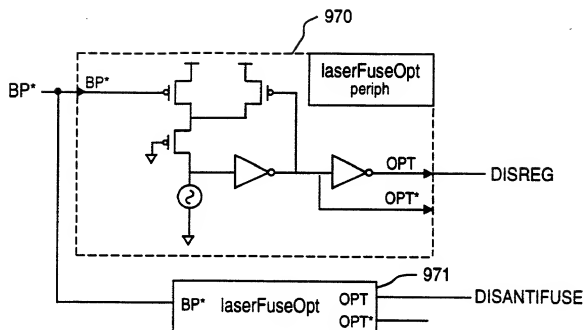


FIG. 59H

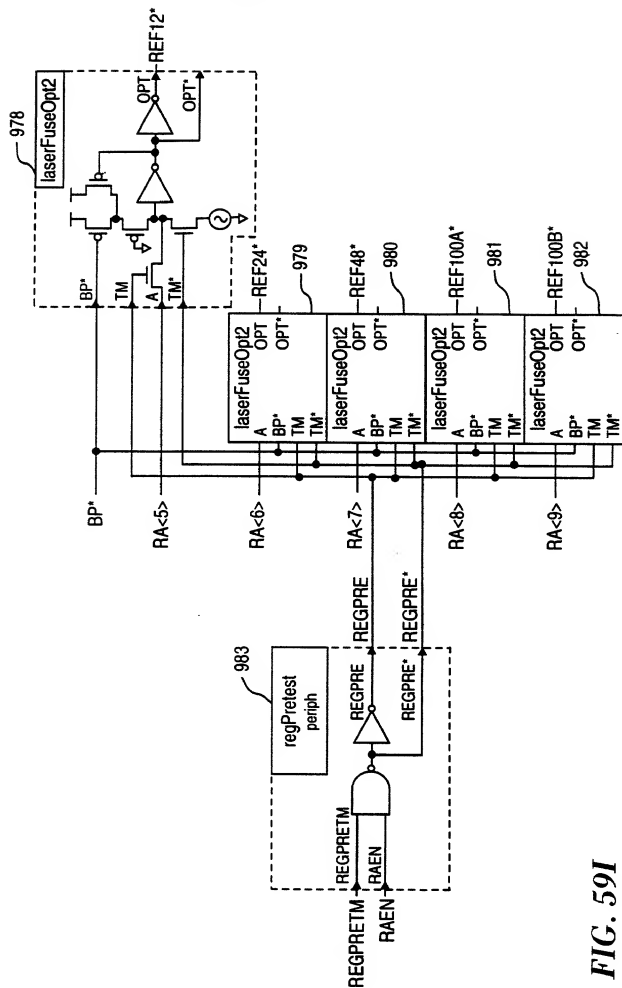
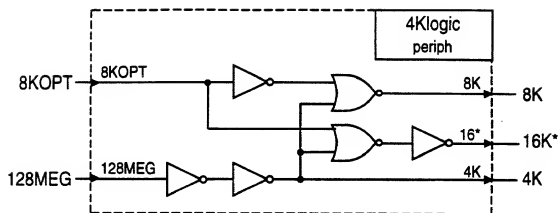
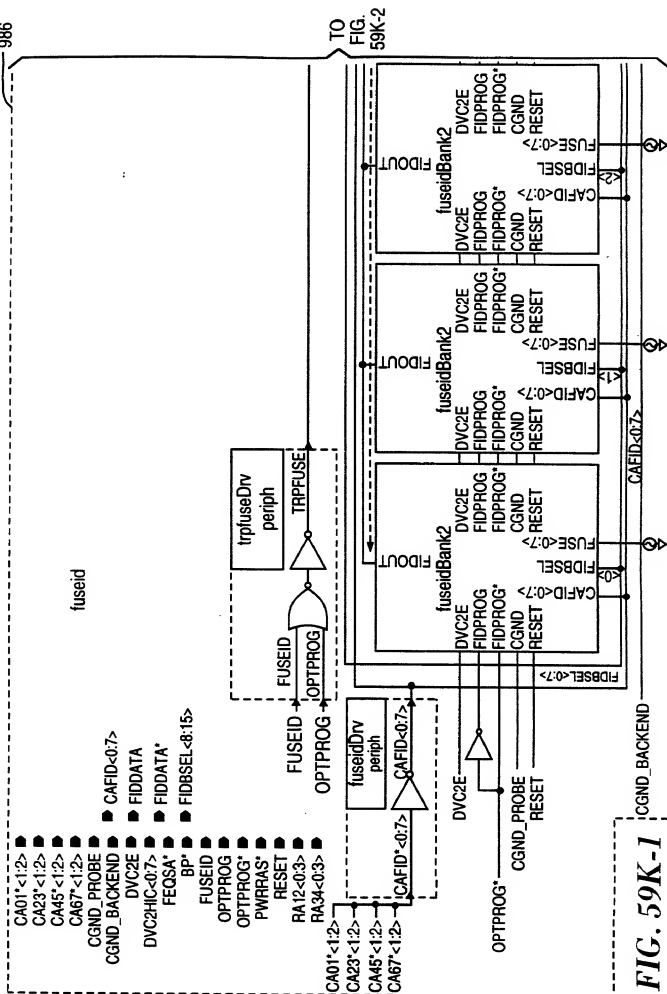


FIG. 59I

**FIG. 59J**



**FIG. 59K-1**

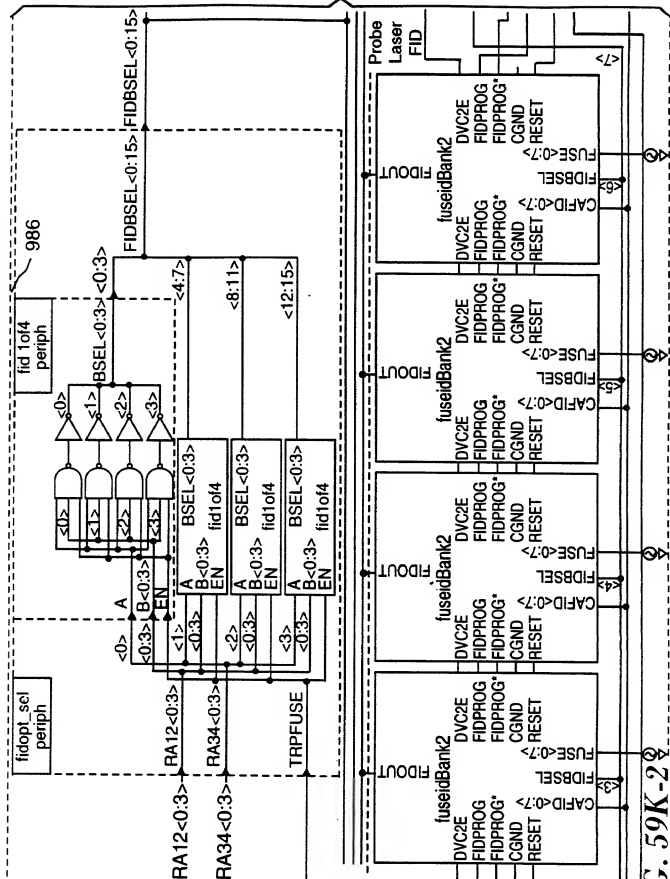


FIG. 59K-2

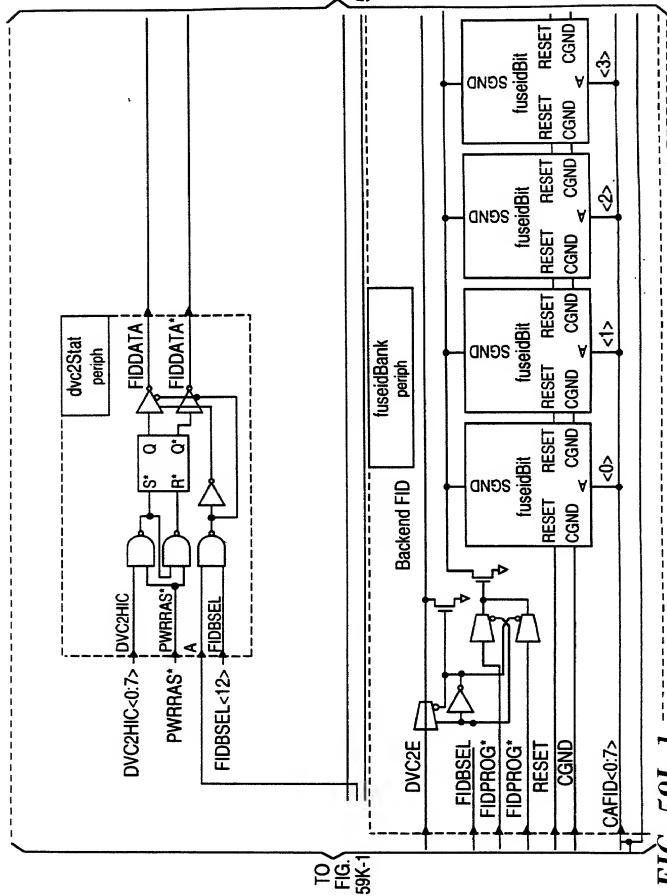
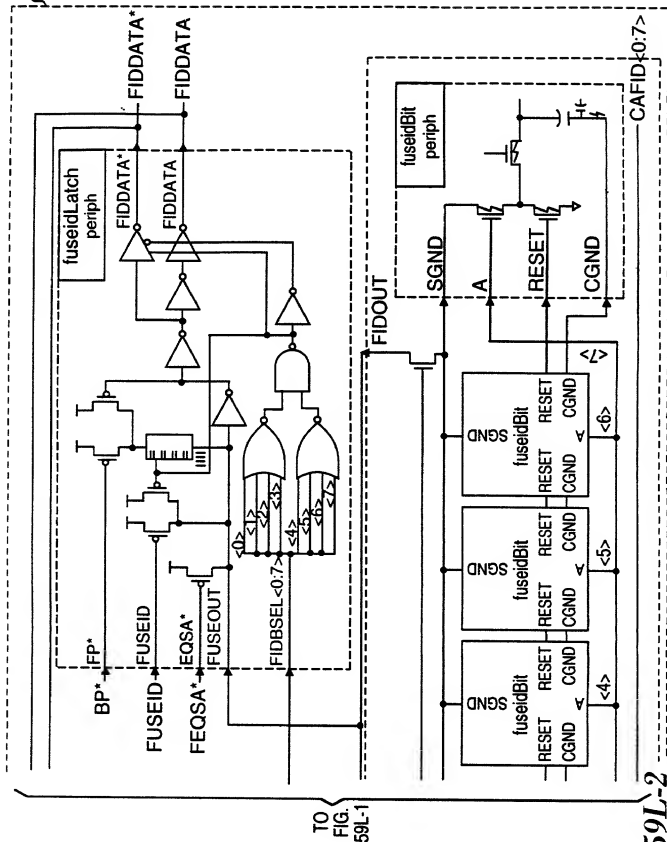
TO  
FIG.  
59L-2TO  
FIG.  
59K-1

FIG. 59L-1





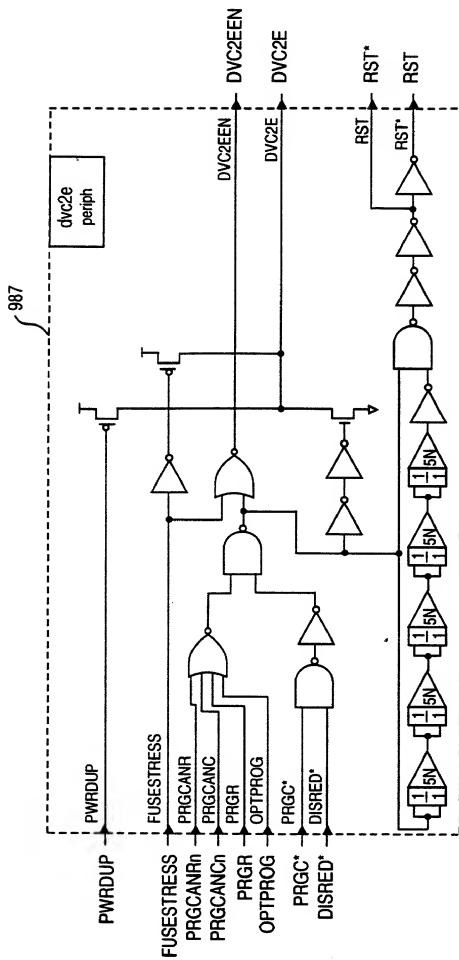
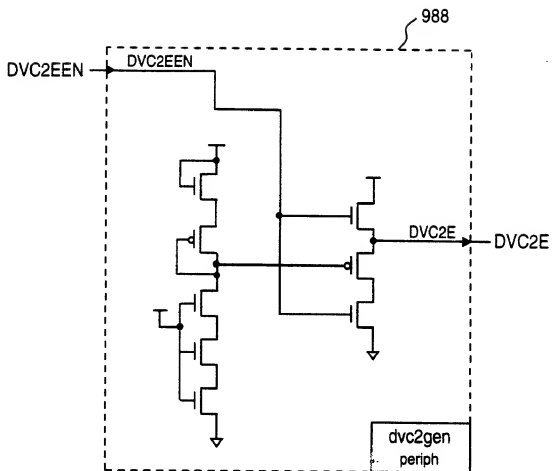
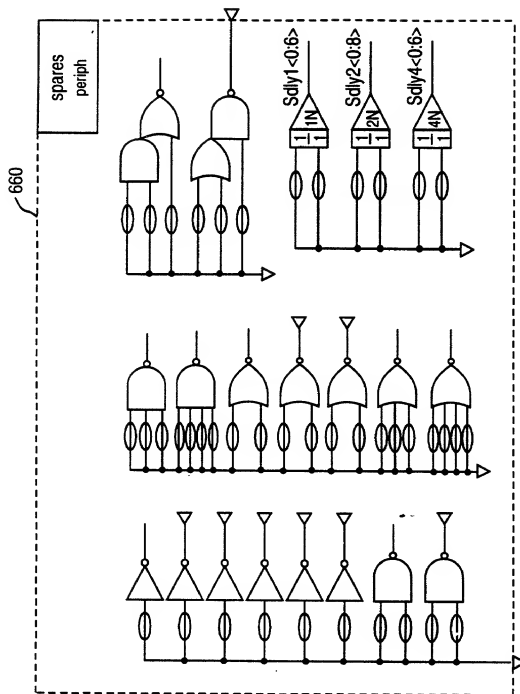


FIG. 59M

**FIG. 59N**





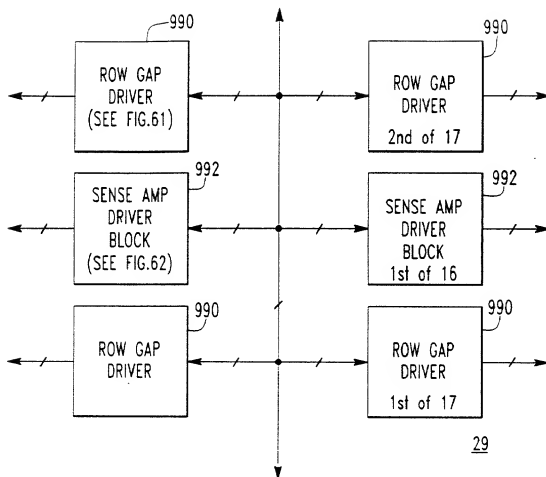


FIG. 60

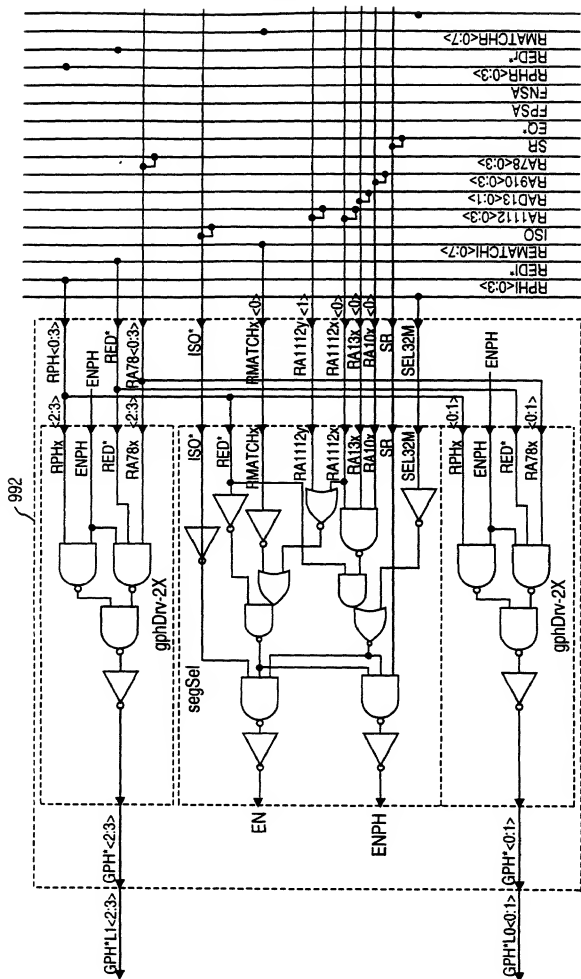


FIG. 61

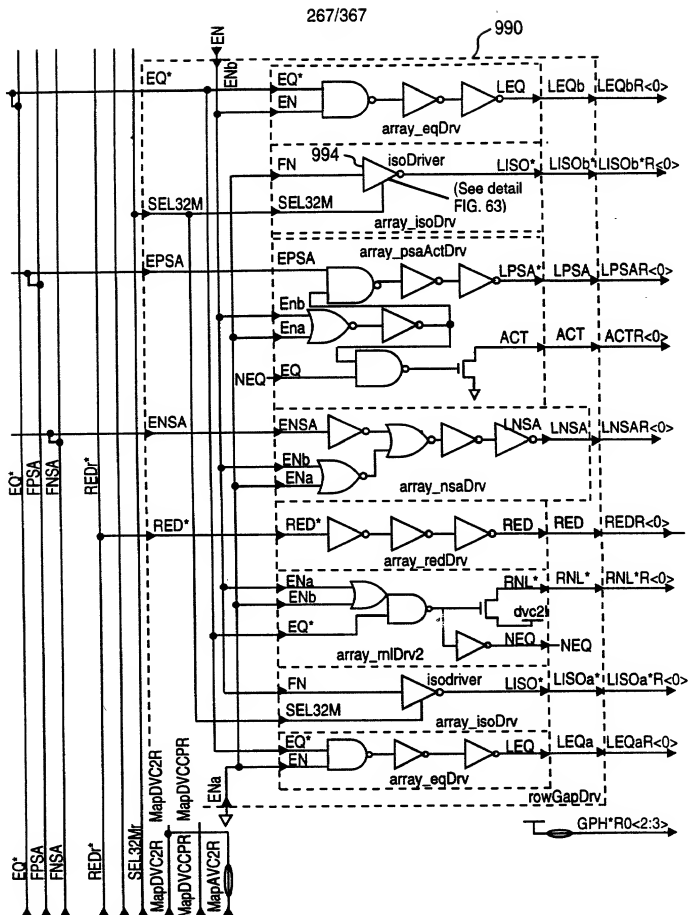


FIG. 62

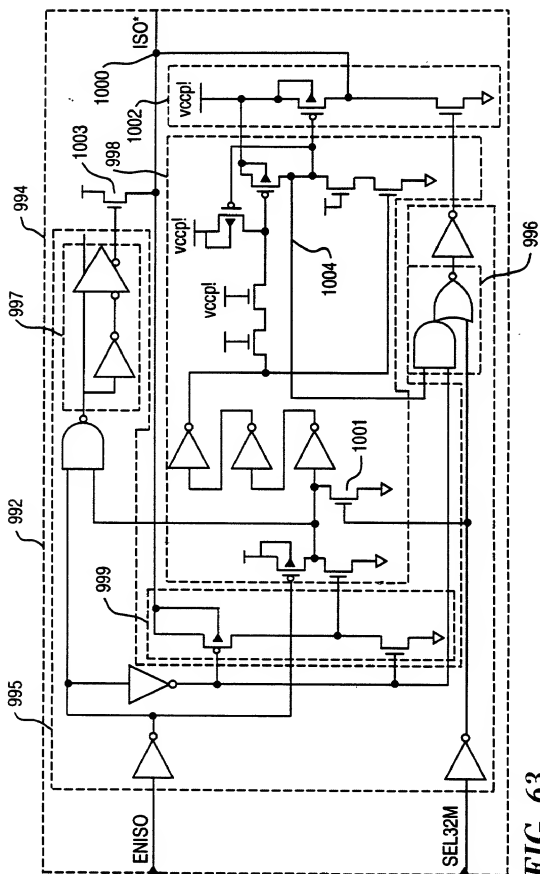


FIG. 63



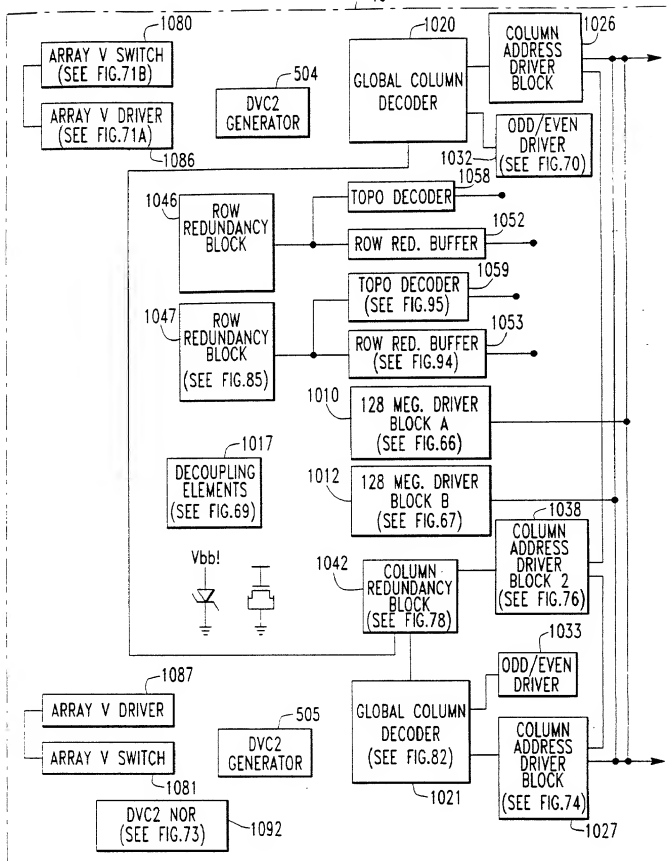


FIG. 64A

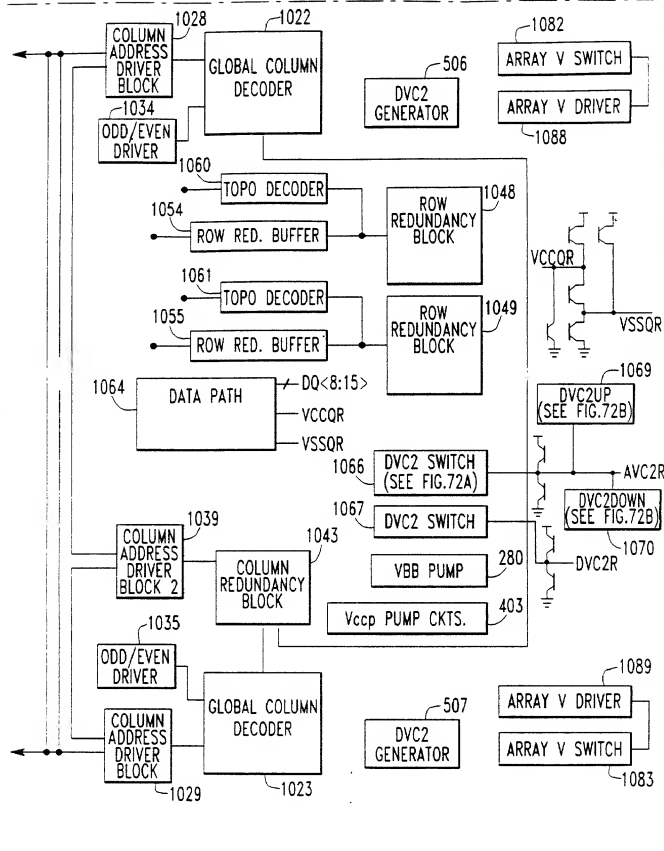


FIG. 64B

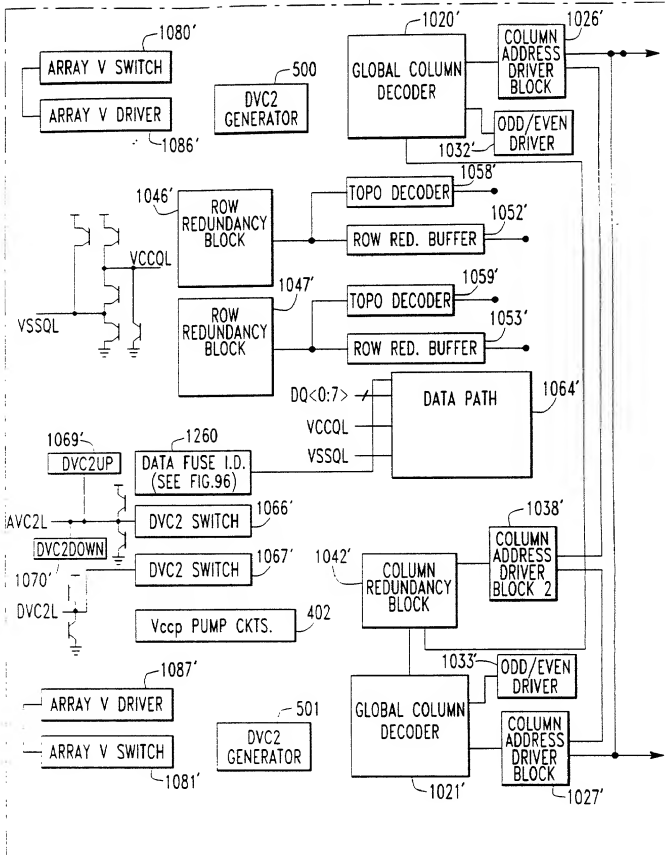


FIG. 65A

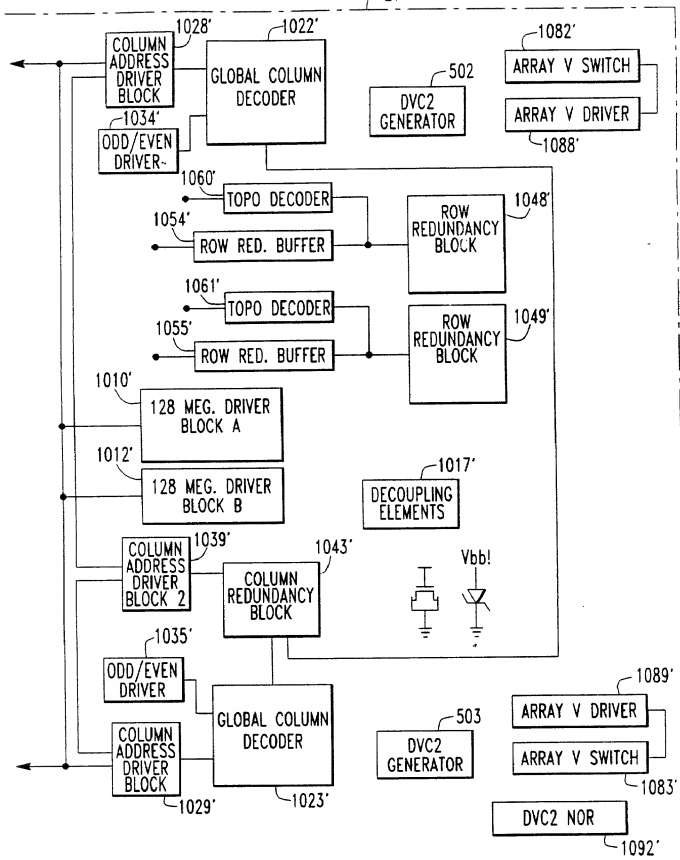
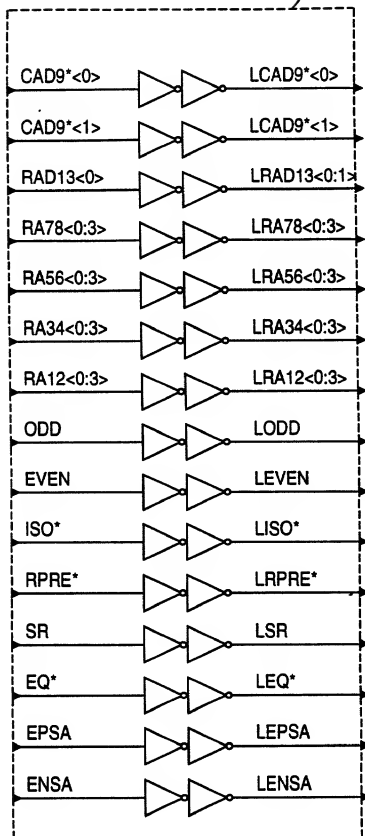


FIG. 65B

**FIG. 66**

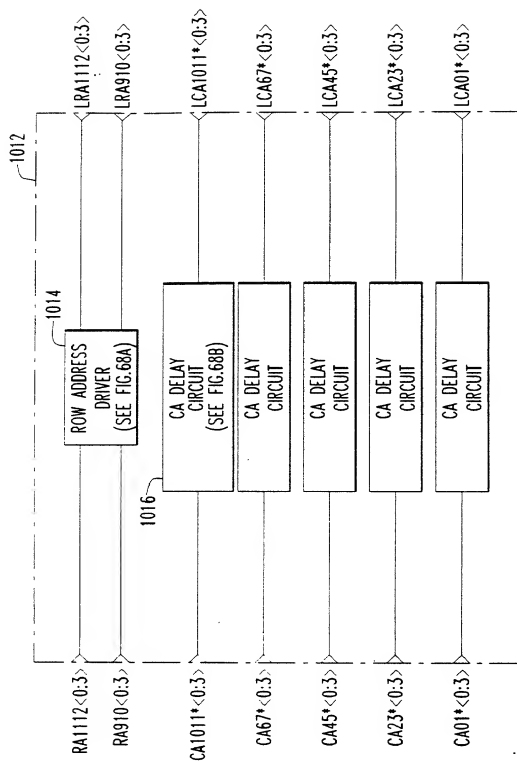
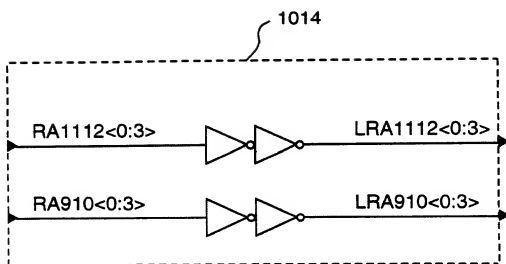
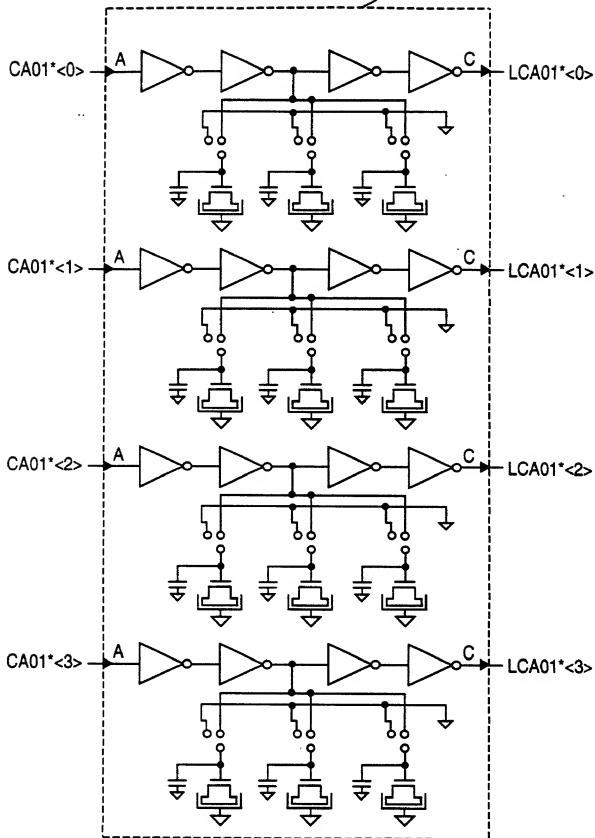
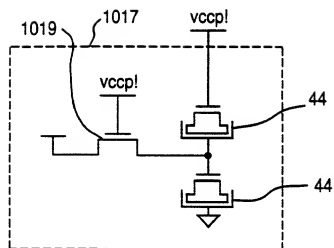


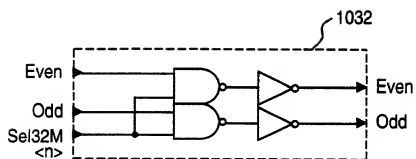
FIG. 67

**FIG. 68A**

**FIG. 68B**



**FIG. 69**

**FIG. 70**

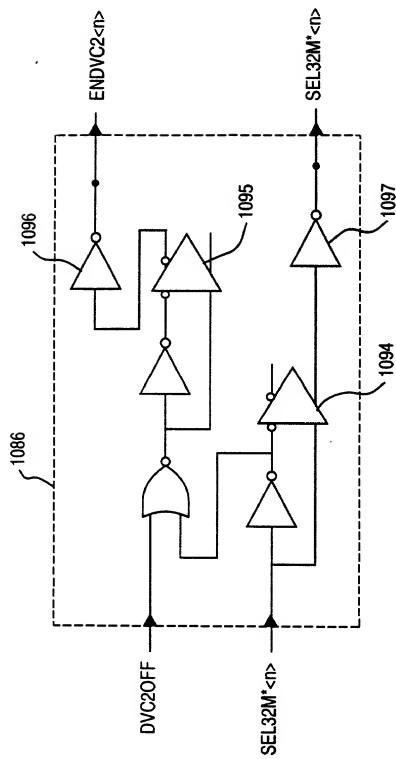
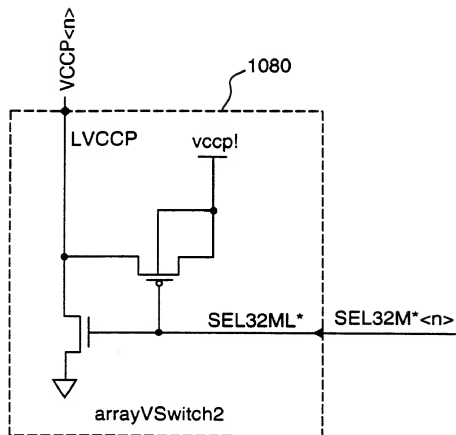


FIG. 71A



**FIG. 71B**

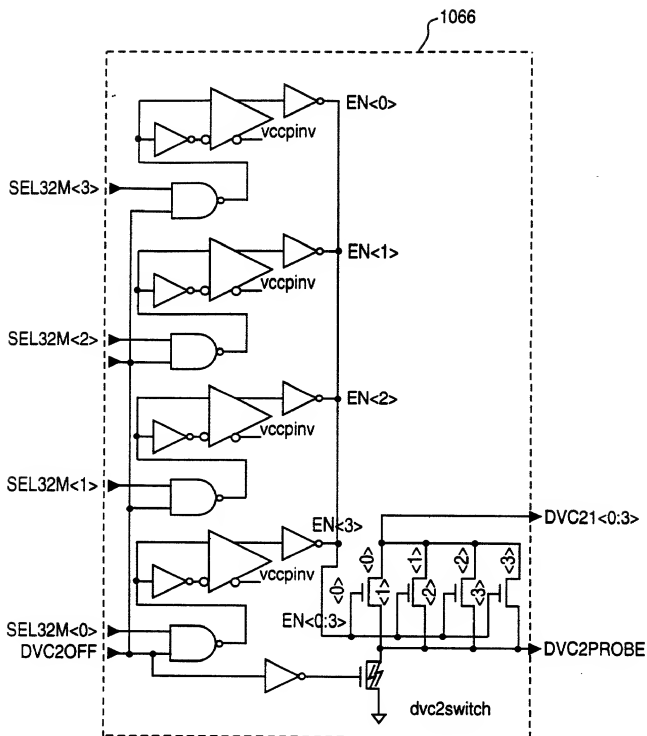
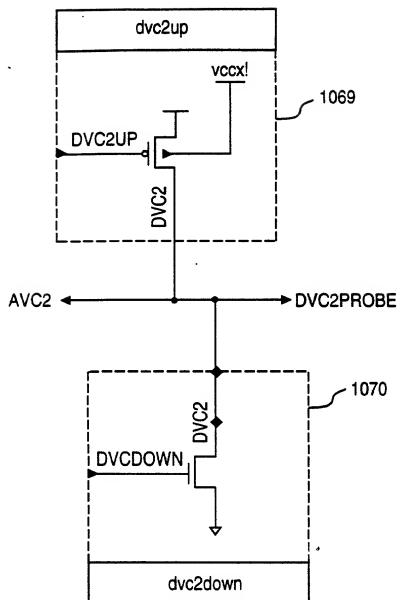
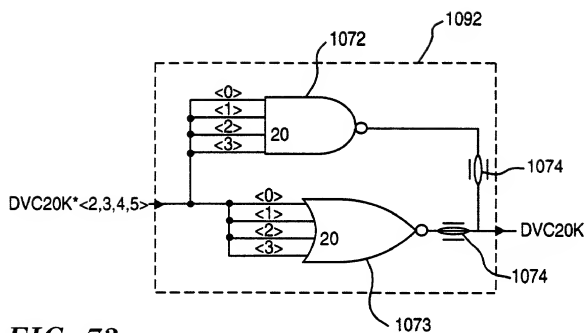


FIG. 72A

**FIG. 72B**

**FIG. 73**

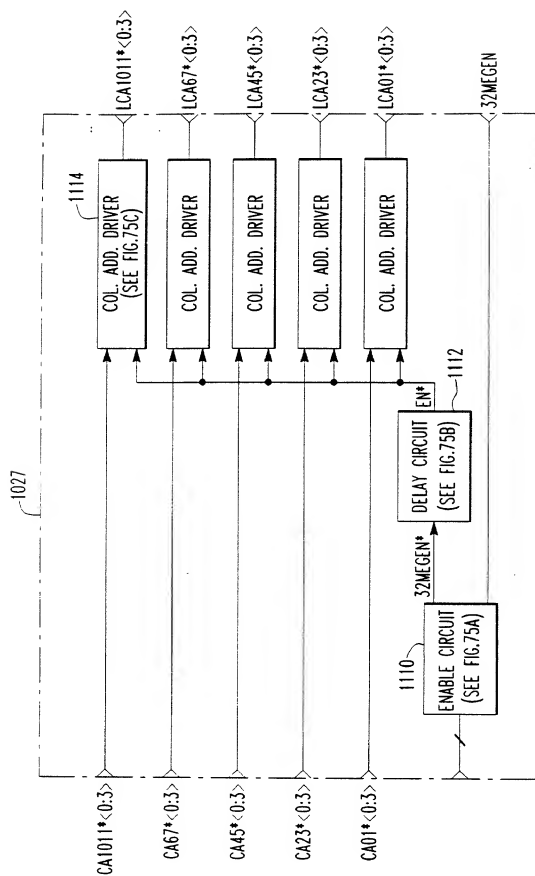
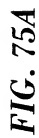


FIG. 74





**FIG. 75A**

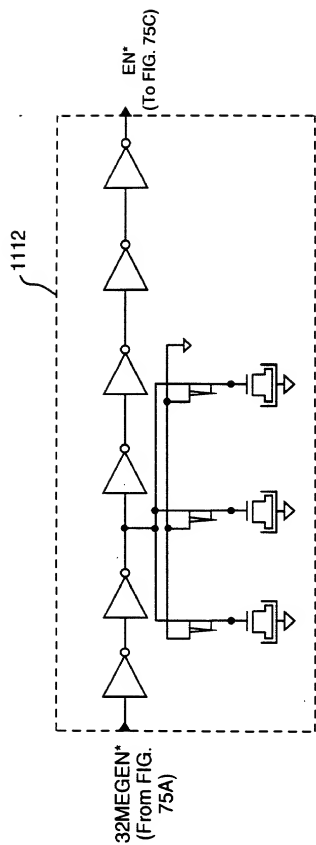


FIG. 75B

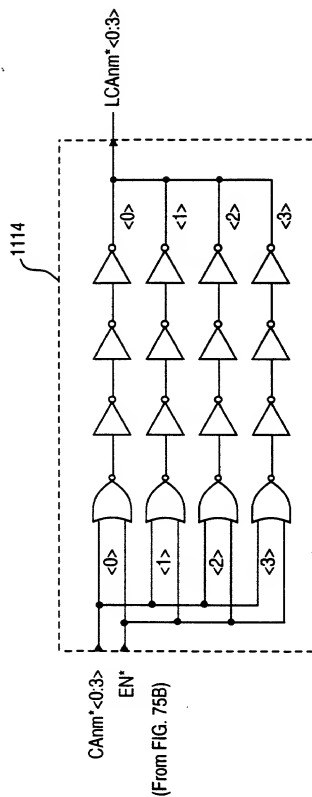


FIG. 75C

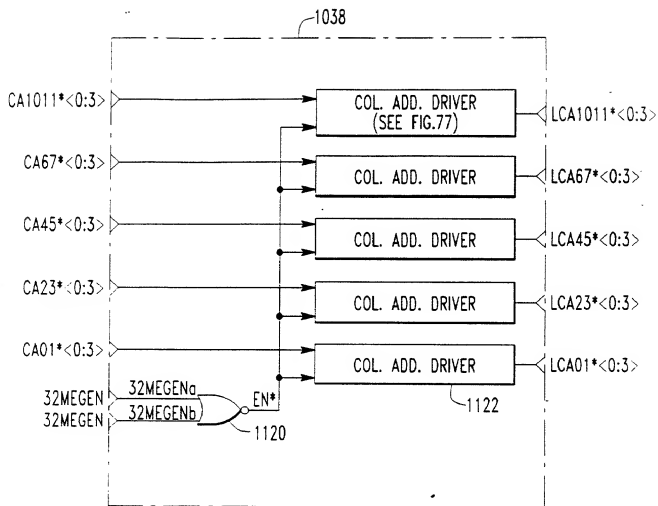
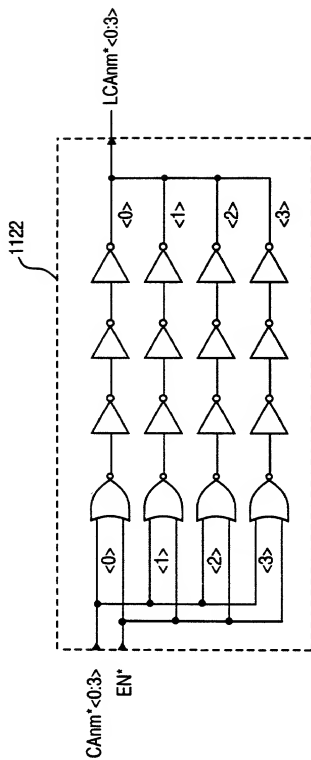


FIG. 76

[illegible]

**FIG. 77**

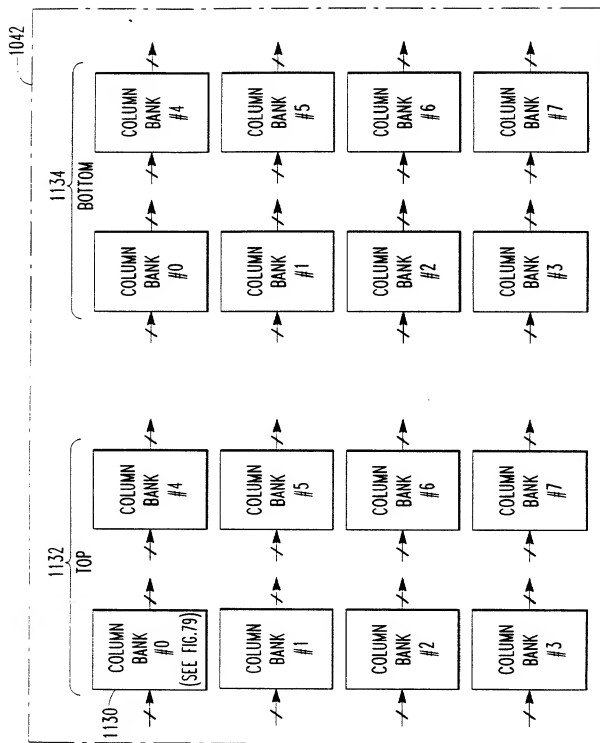


FIG. 78

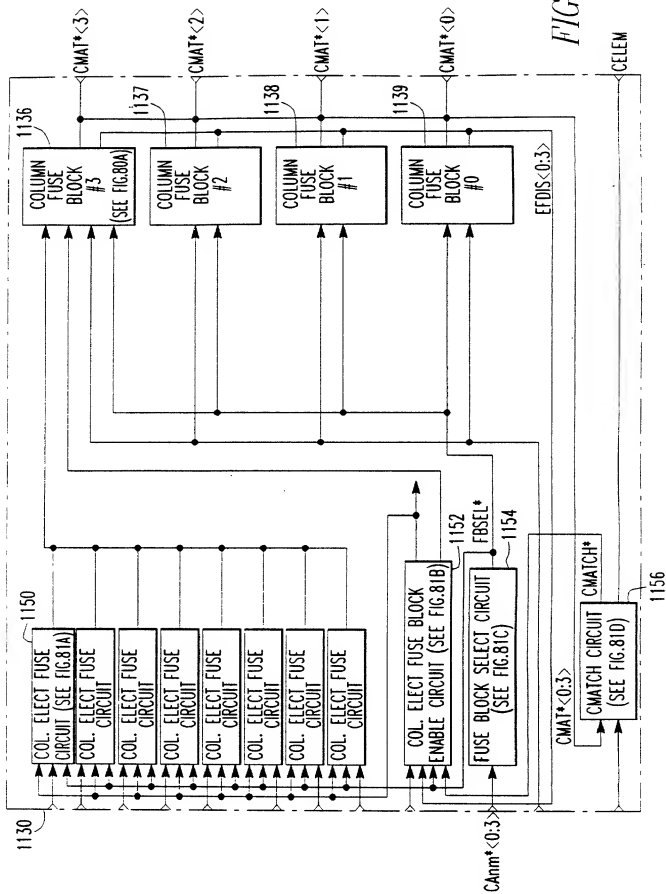


FIG. 79

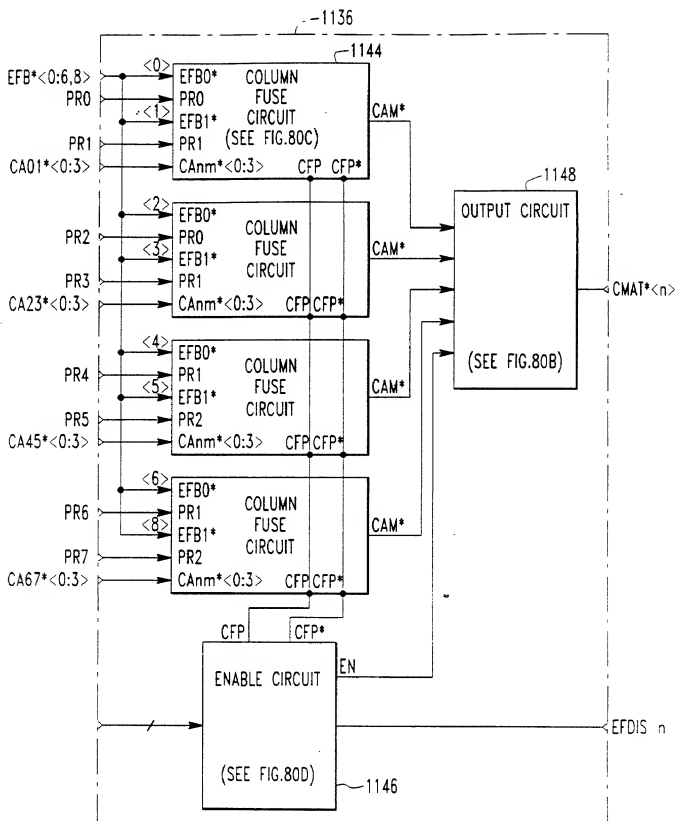
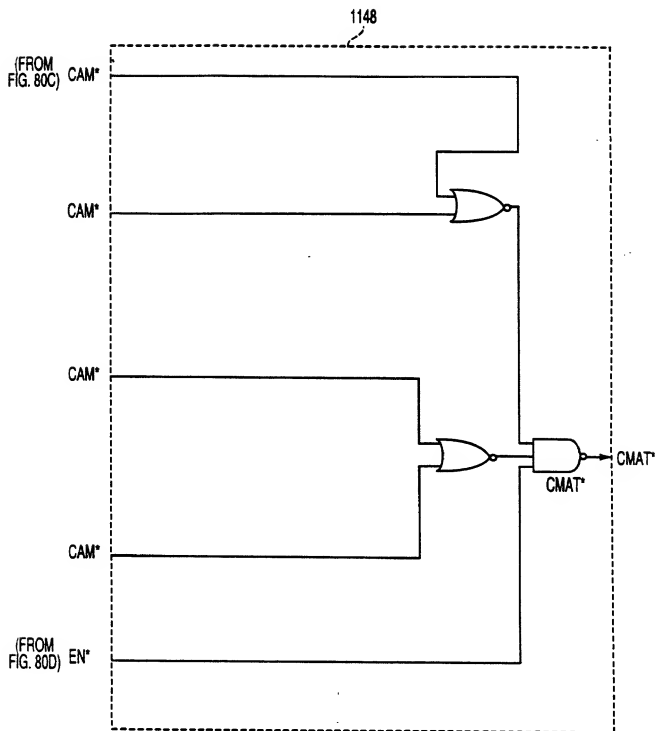


FIG. 80A



**FIG. 80B**

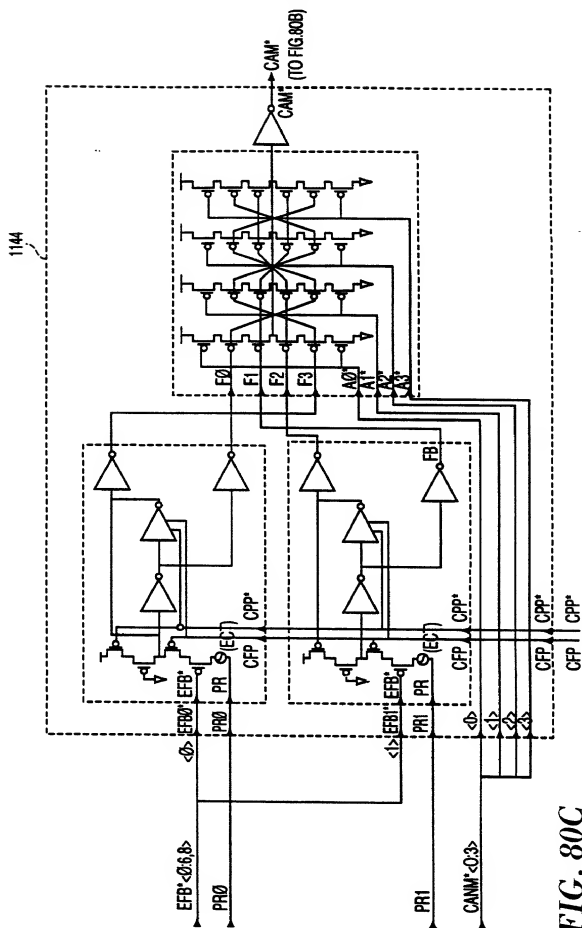


FIG. 80C

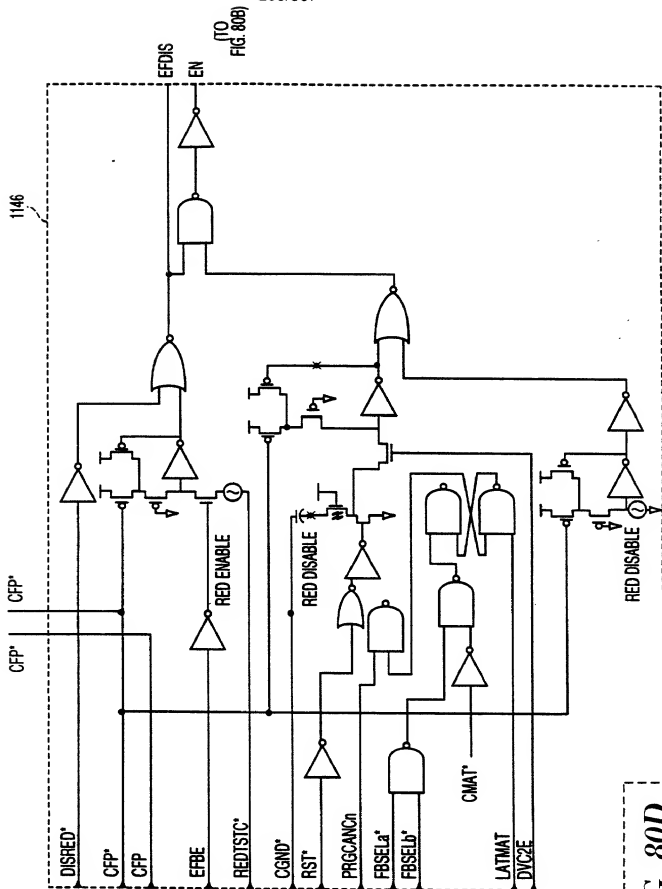
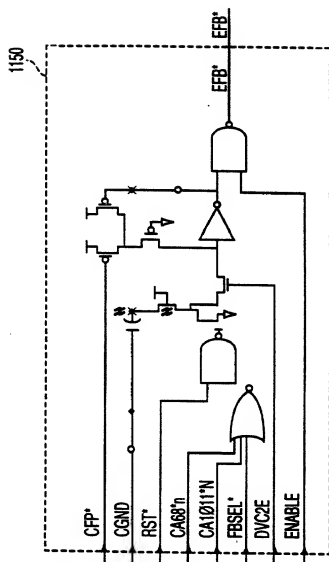


FIG. 80D



**FIG. 81A**

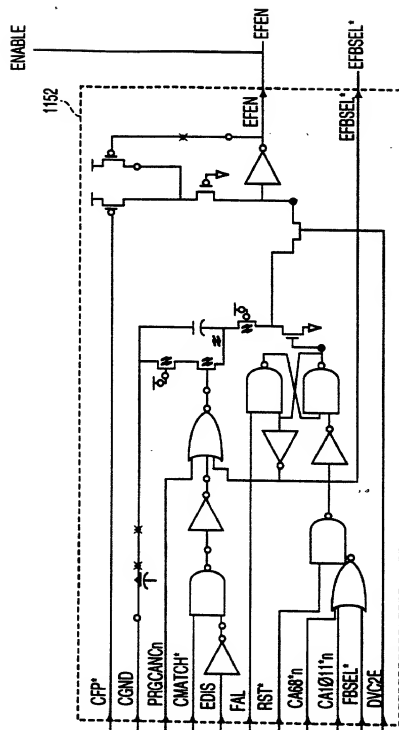
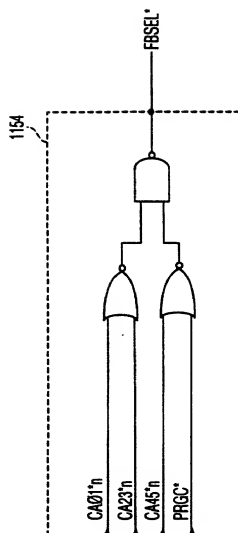


FIG. 81B

*FIG. 81C*

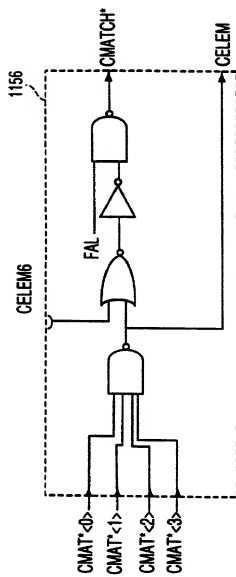


FIG. 81D

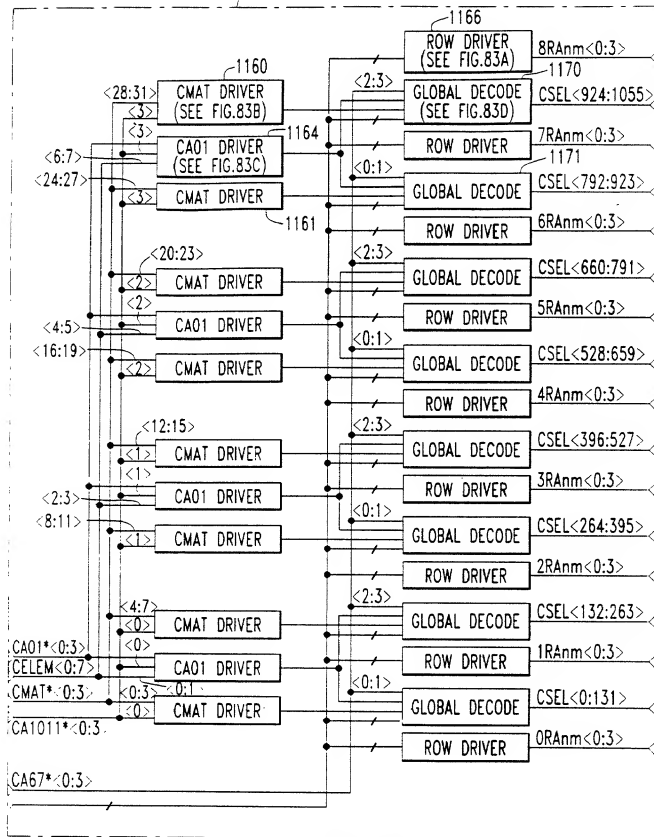


FIG. 82



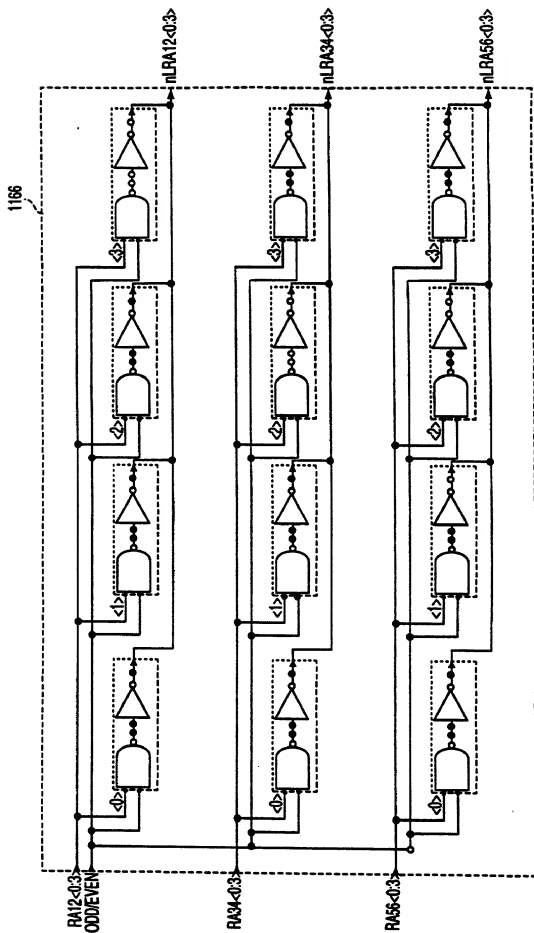


FIG. 83A

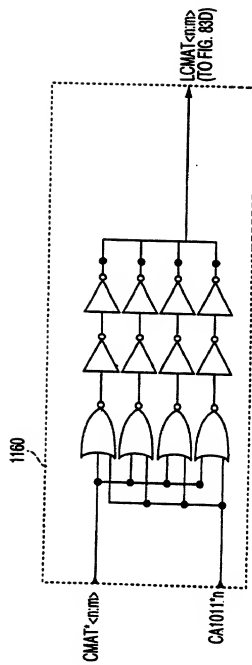


FIG. 83B

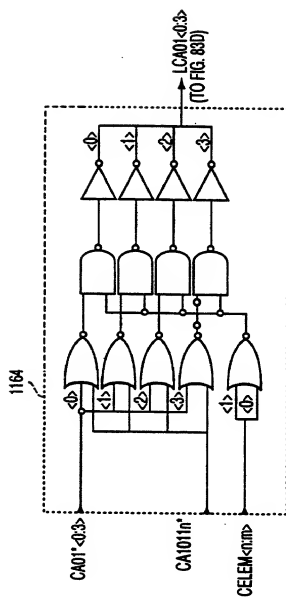
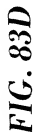


FIG. 83C



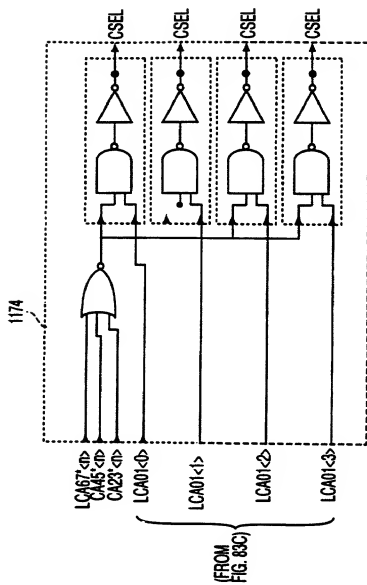
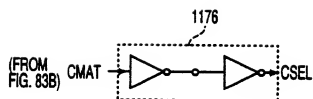


FIG. 84A

**FIG. 84B**

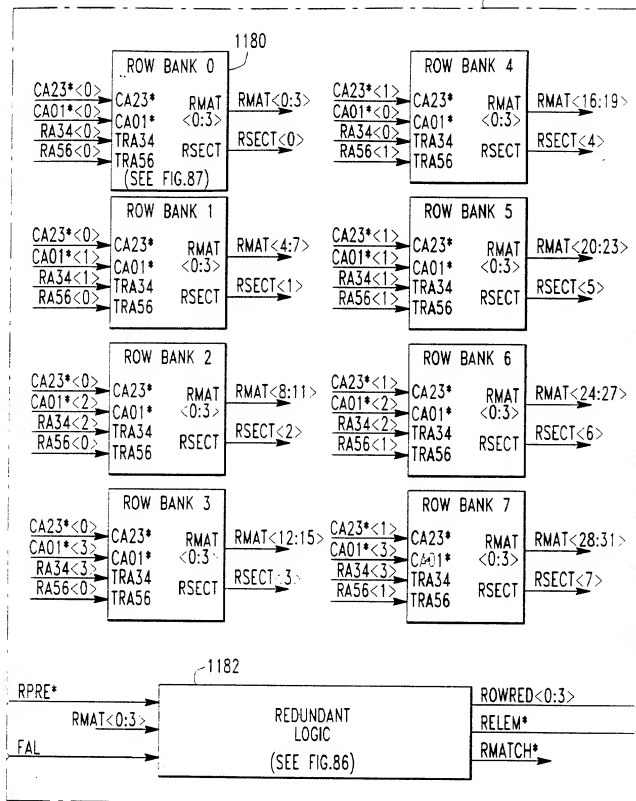


FIG. 85

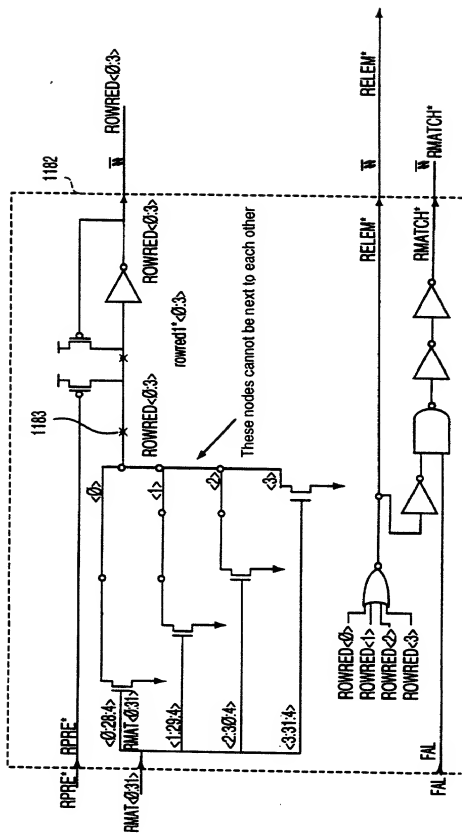
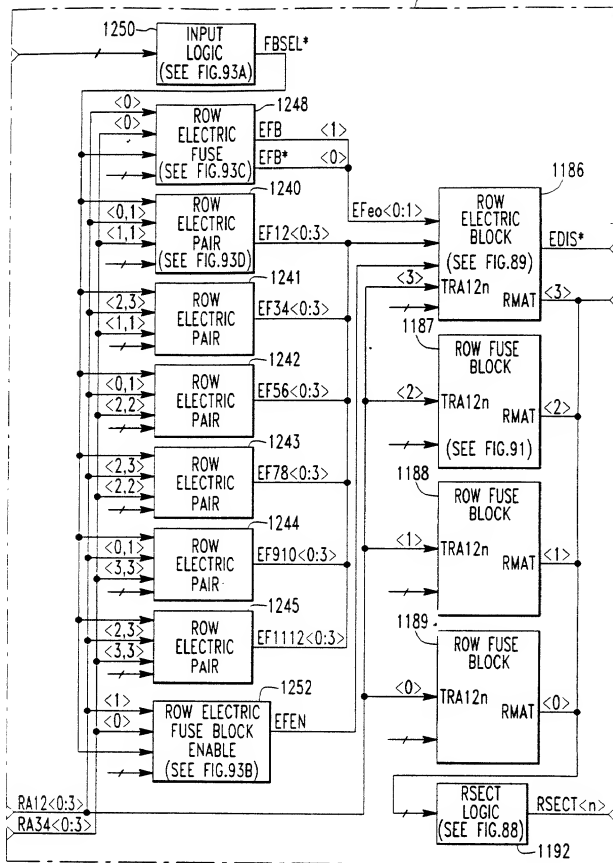
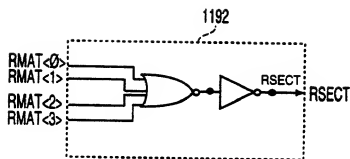


FIG. 86





**FIG. 88**

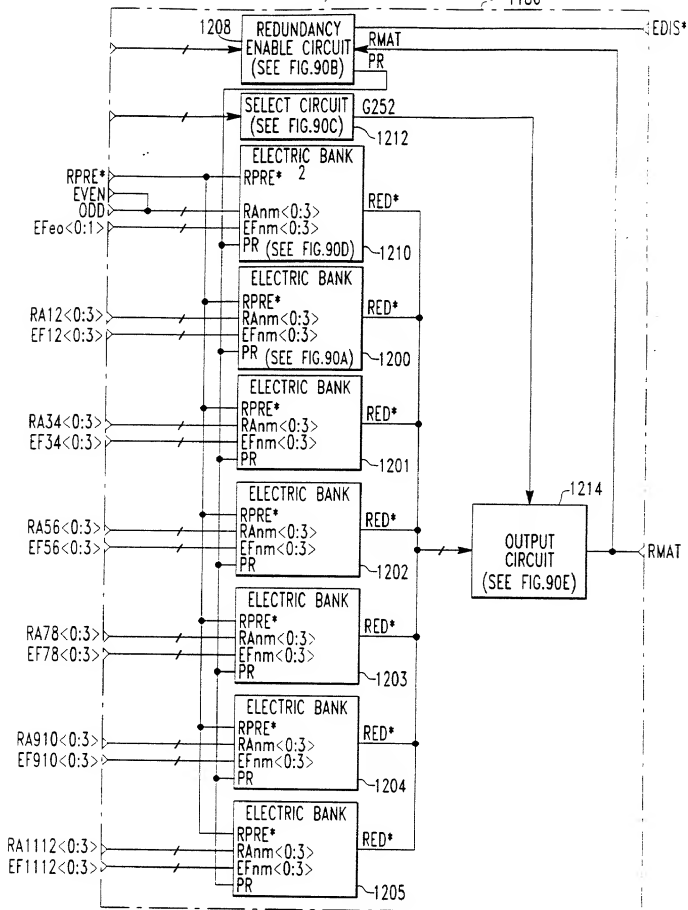


FIG. 89

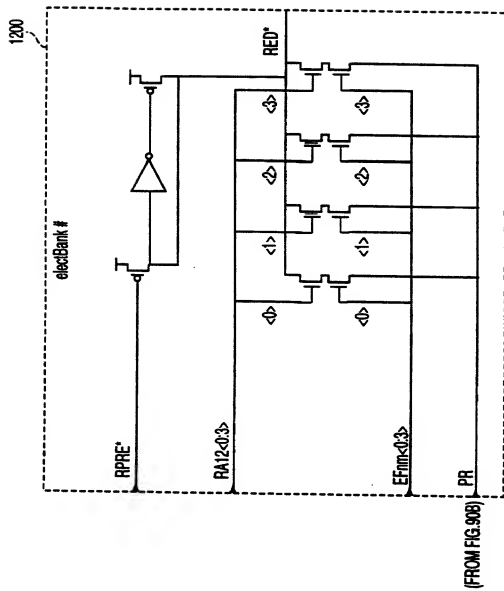


FIG. 90A

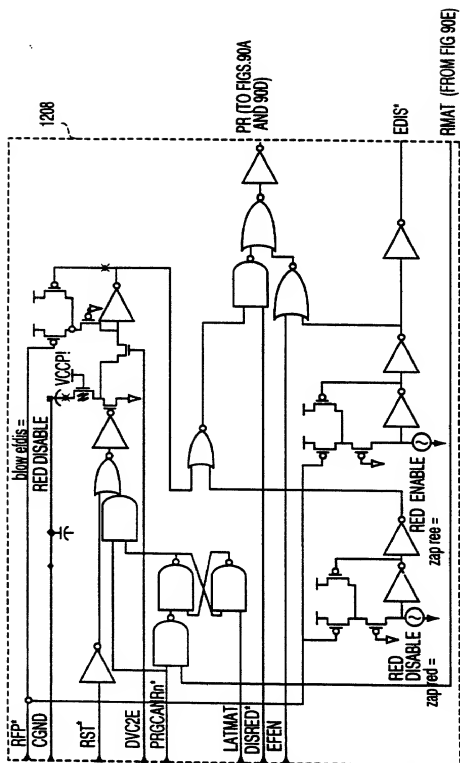
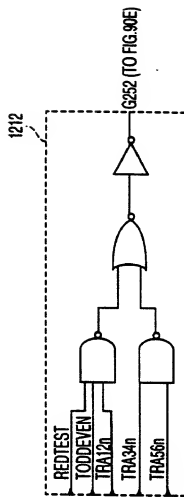


FIG. 90B

**FIG. 90C**



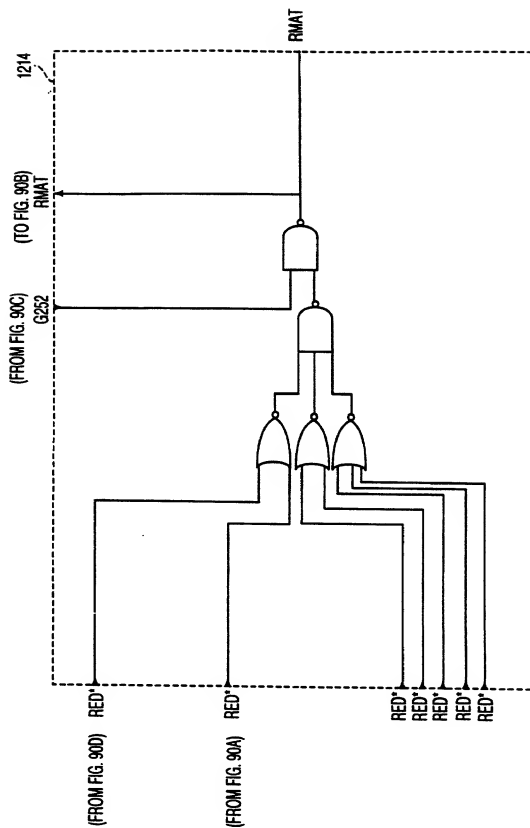


FIG. 90E



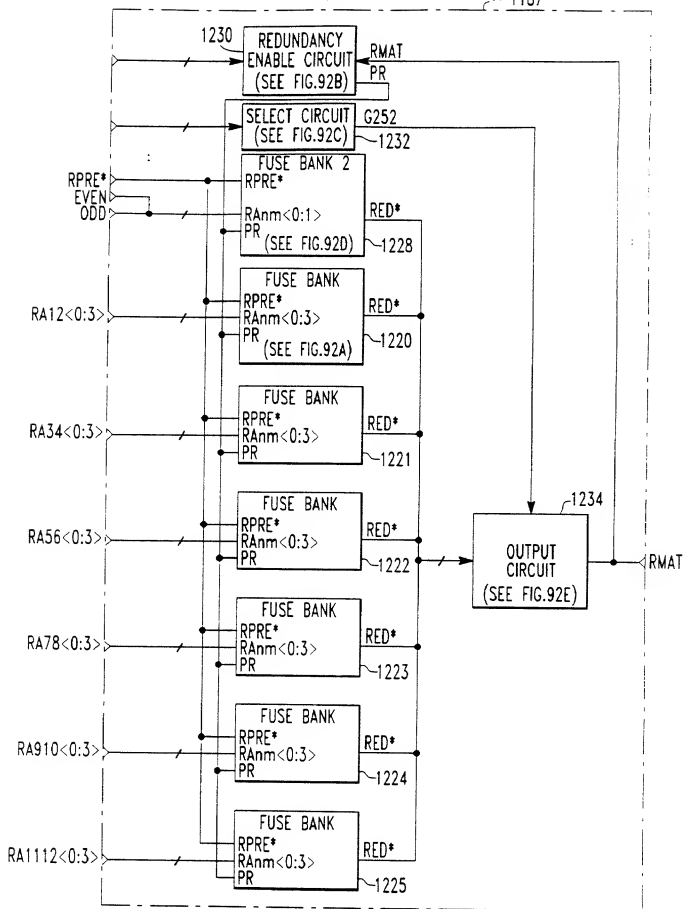


FIG. 91

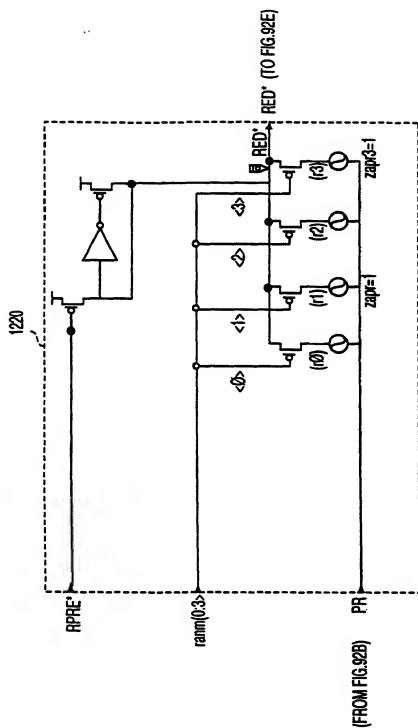
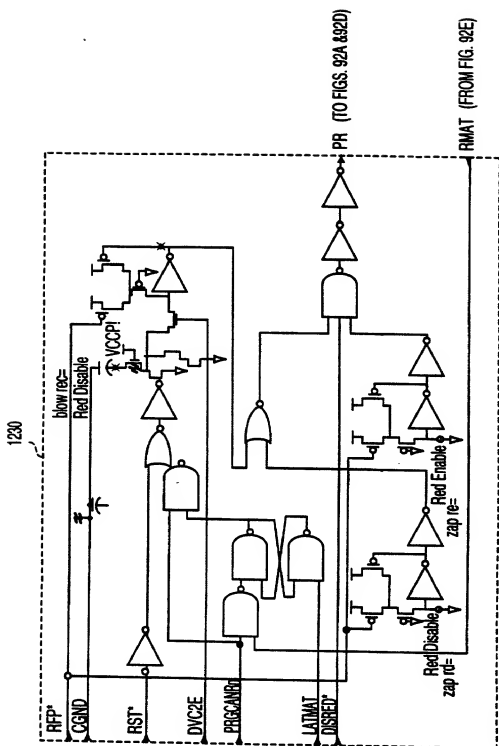


FIG. 92A



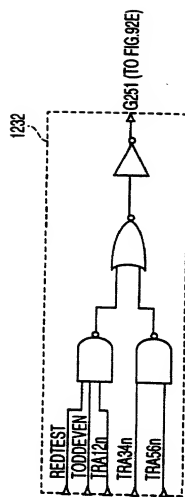


FIG. 92C

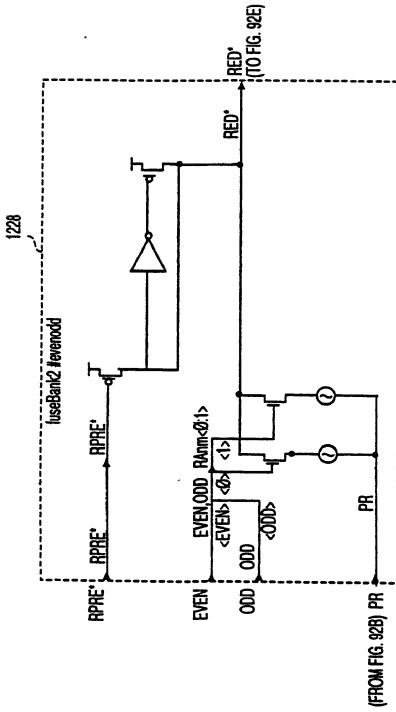


FIG. 92D

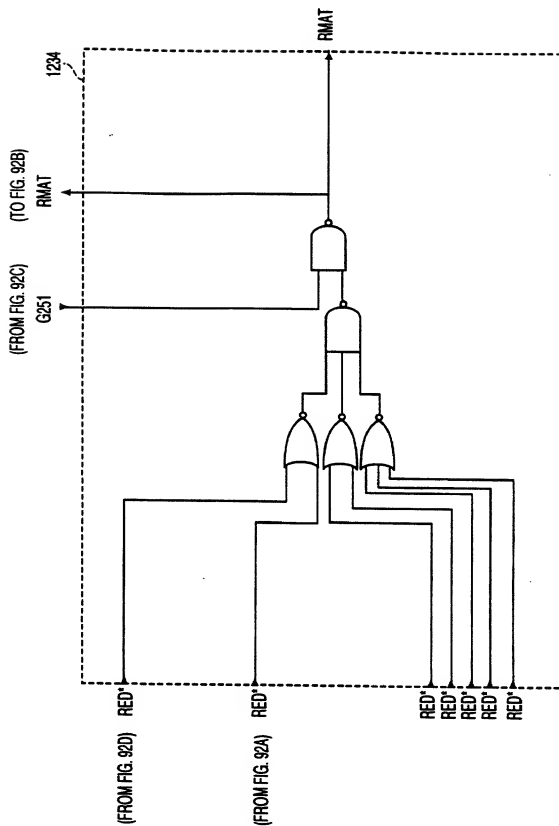
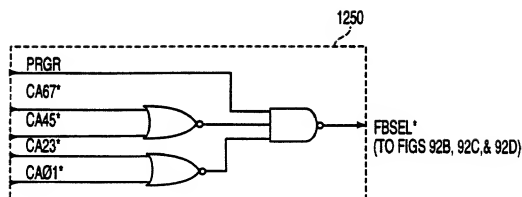


FIG. 92E

**FIG. 93A**



**FIG. 93B**



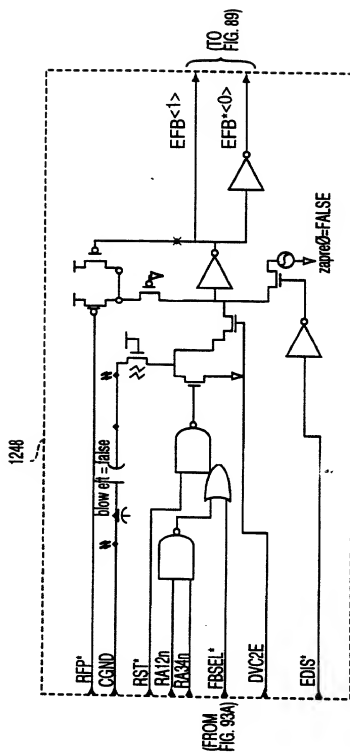


FIG. 93C

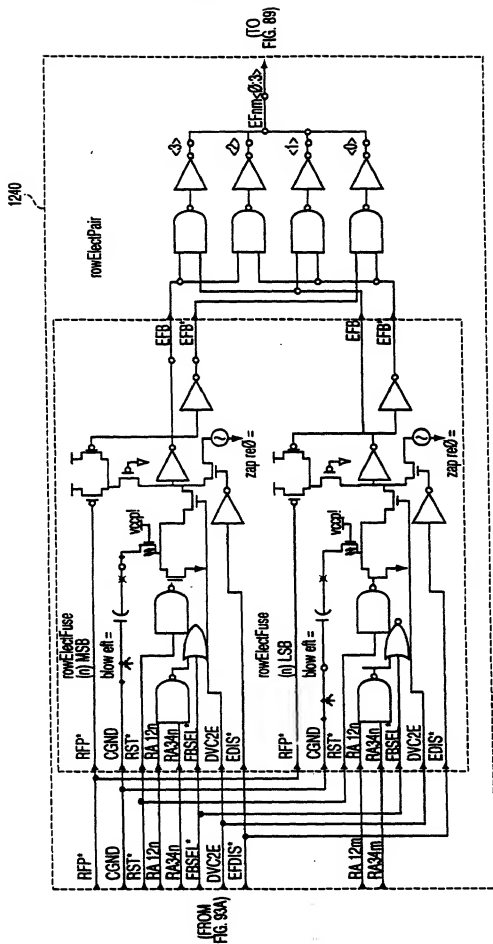
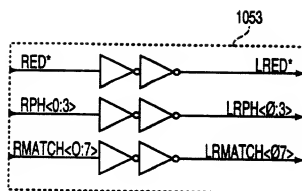


FIG. 93D

**FIG. 94**

1059

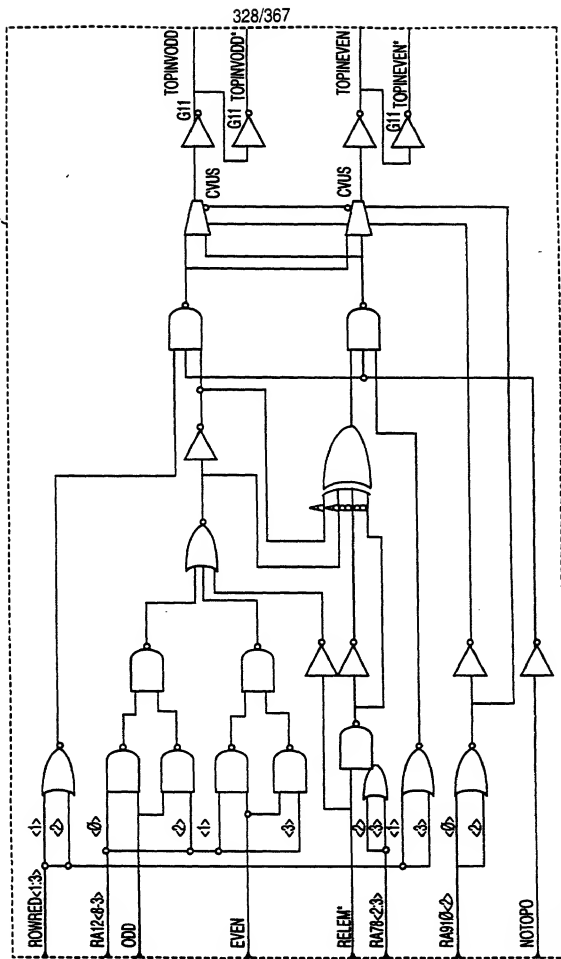


FIG. 95

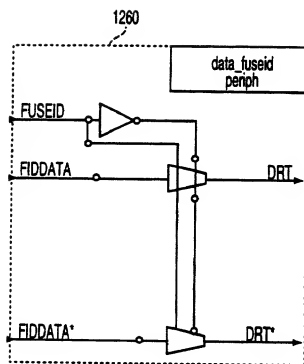
**FIG. 96**



FIG. 97-1 | FIG. 97-2

**FIG. 97-1**

108290\*68223860

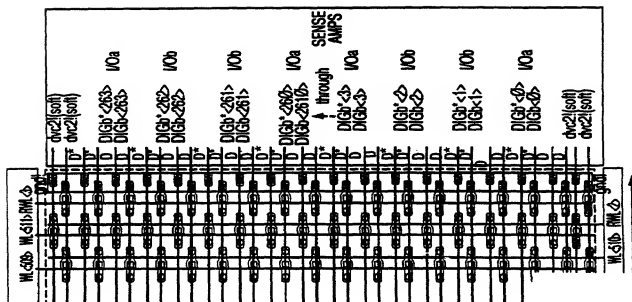
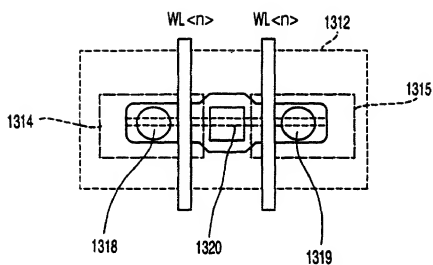


FIG. 97-1 | FIG. 97-2

FIG. 97-2

**FIG. 98**



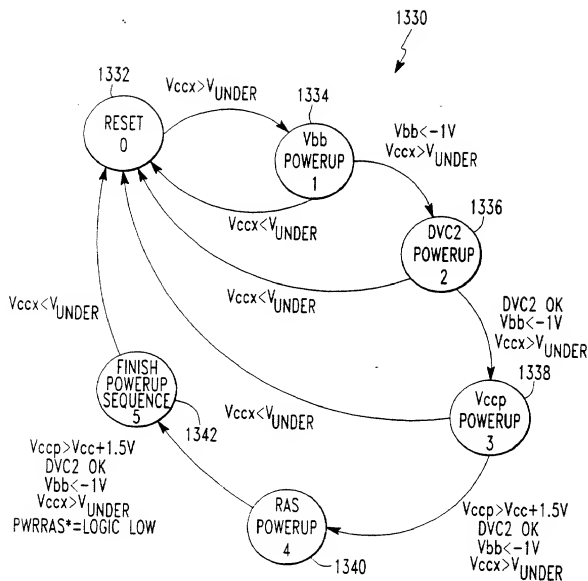
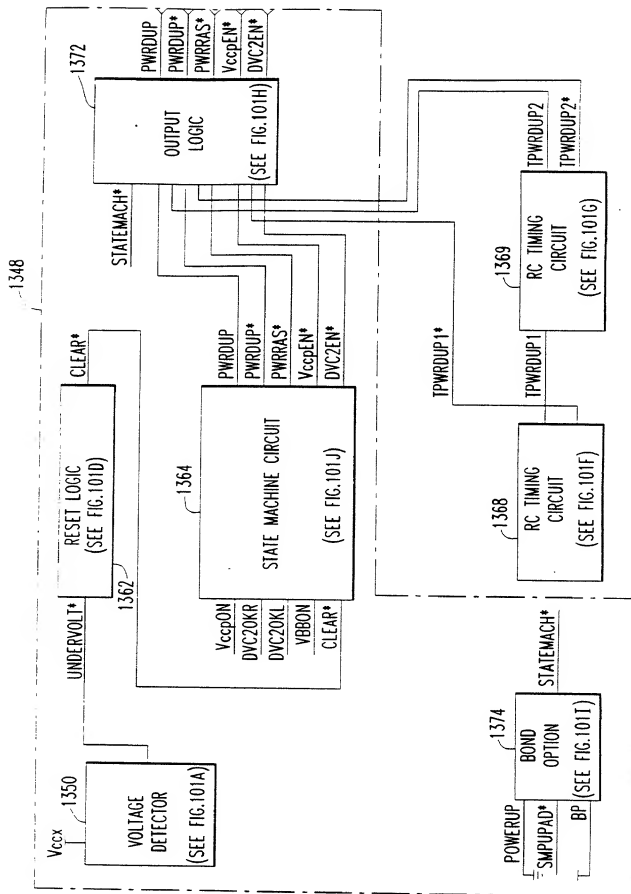


FIG. 99



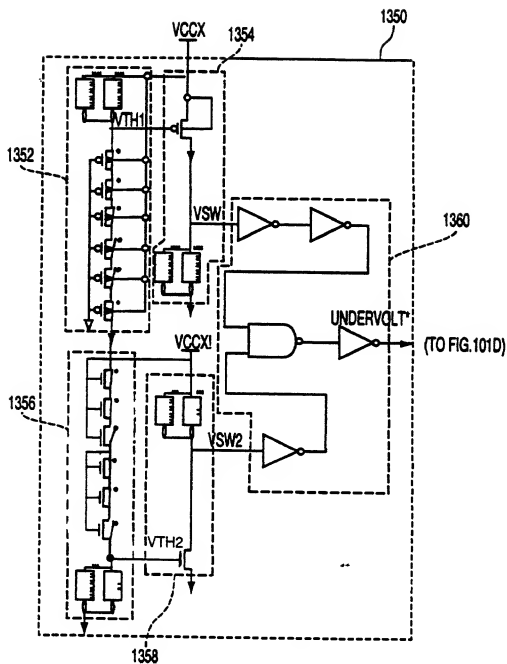
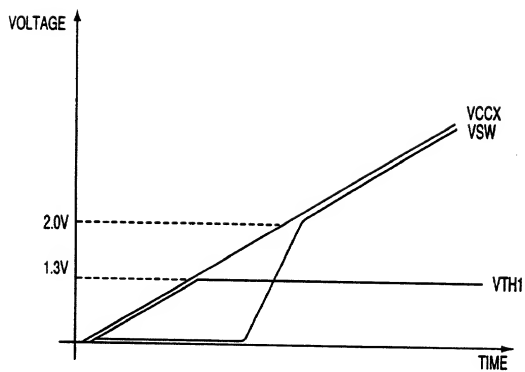
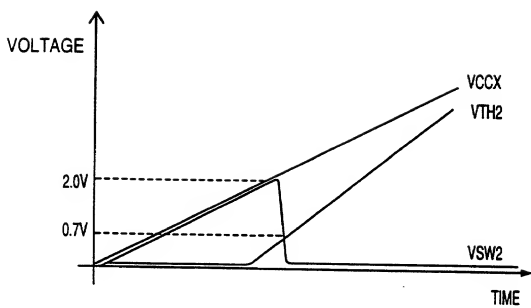
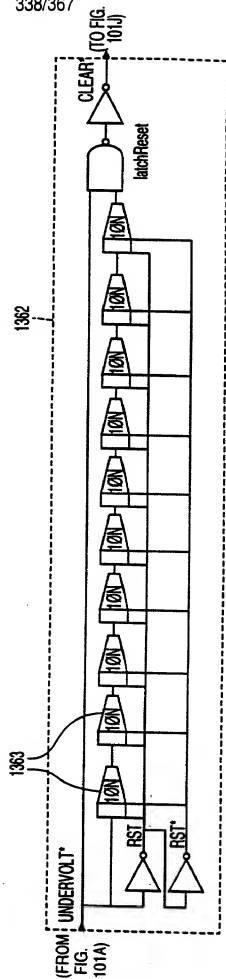


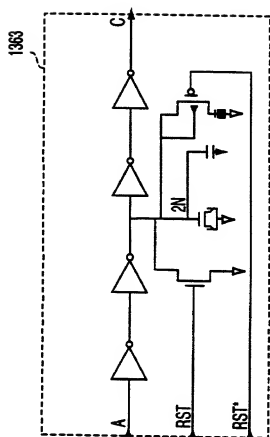
FIG. 101A

**FIG. 101B**

**FIG. 101C**



**FIG. 101D**

**FIG. 101E**

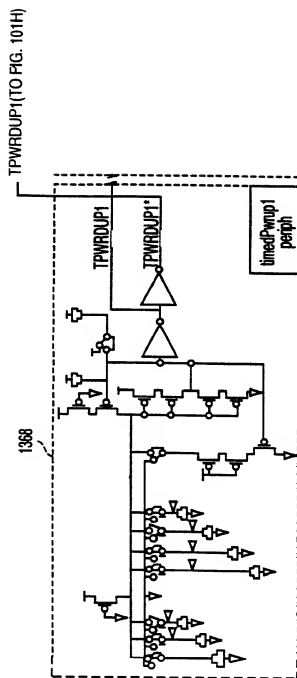


FIG. 101F



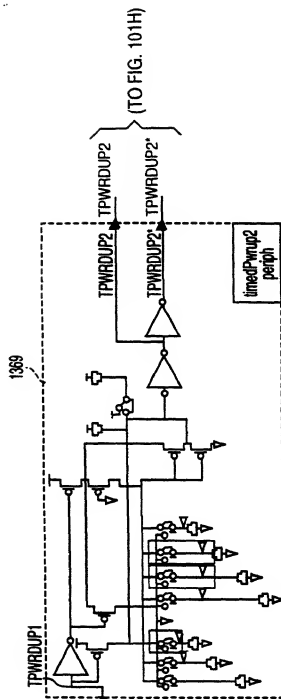
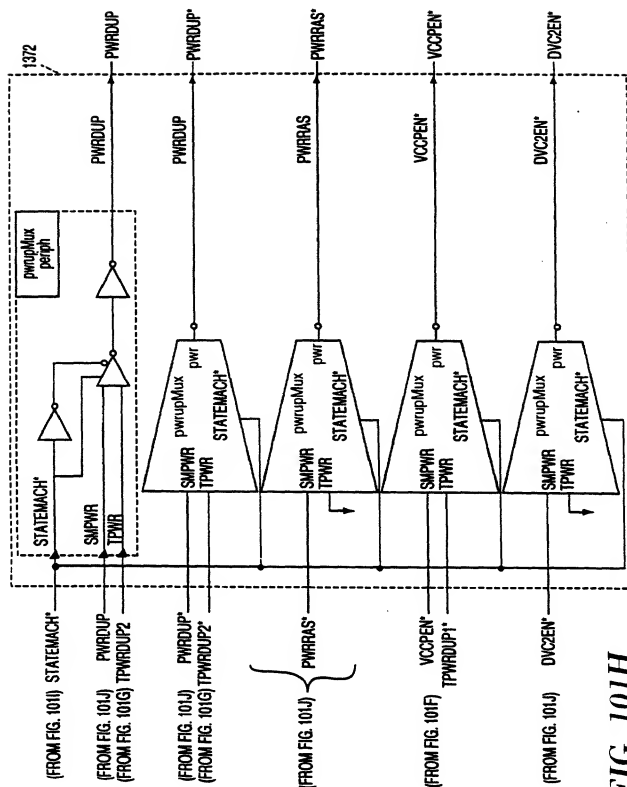


FIG. 101G



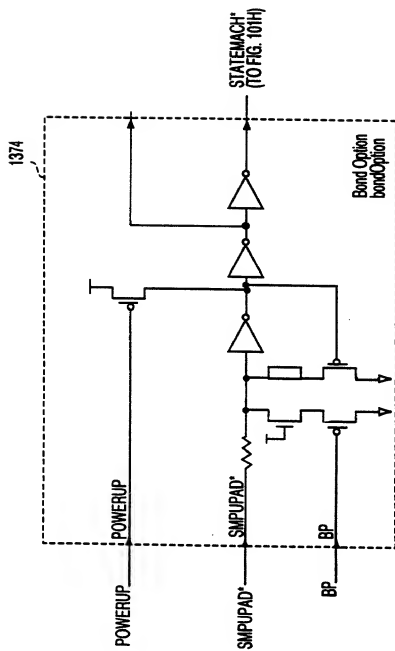
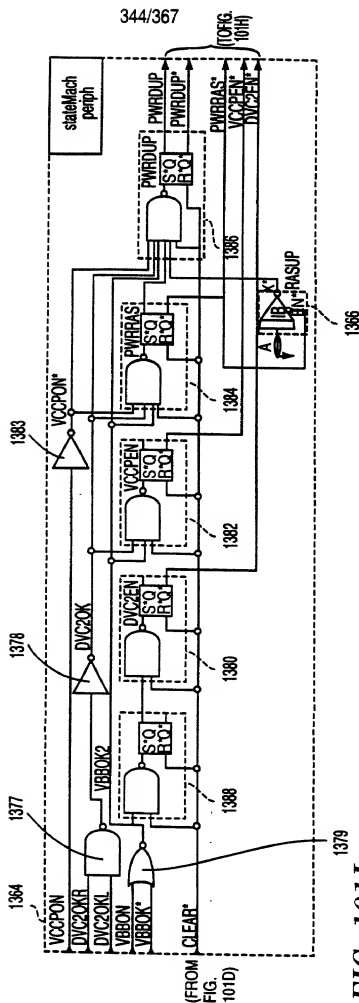
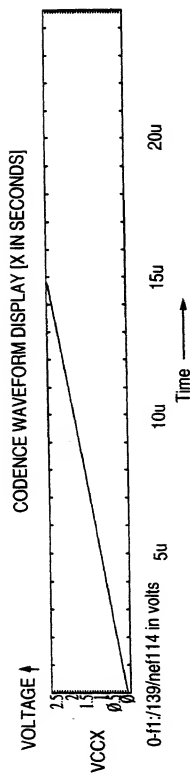


FIG. 10H

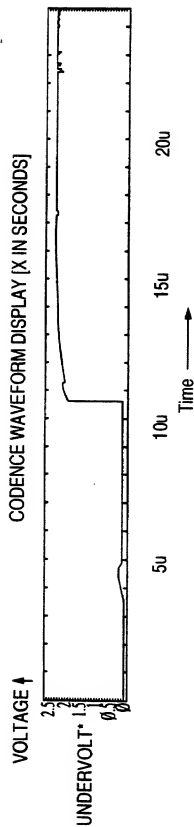


**FIG. 101J**



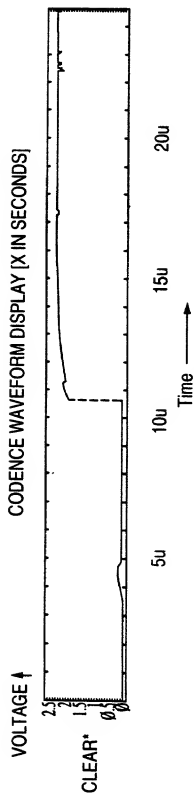
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102A**



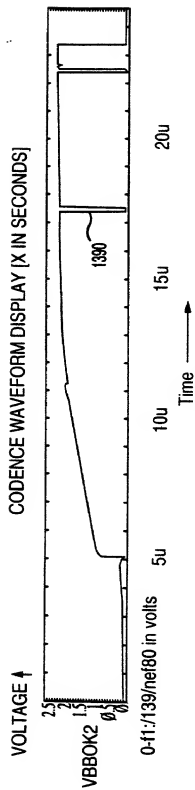
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102B**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

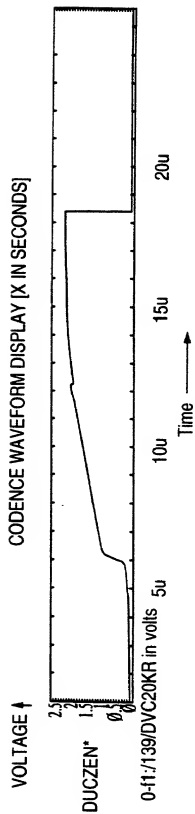
**FIG. 102C**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

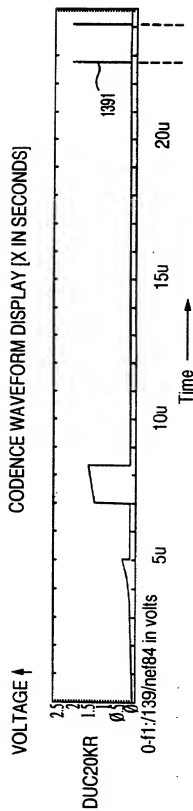
**FIG. 102D**





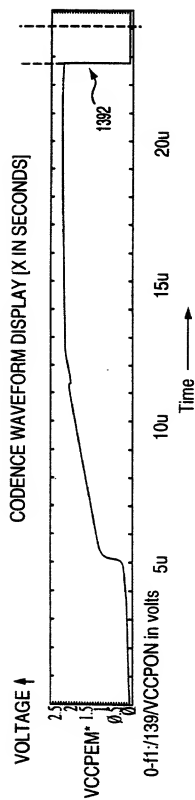
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102E**



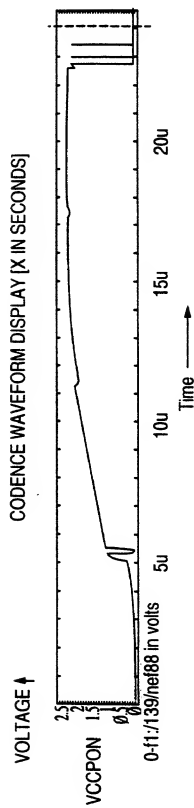
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102F**



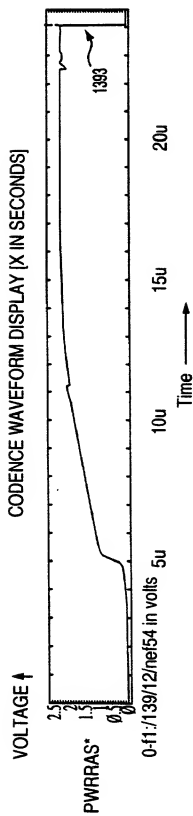
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

FIG. 102C



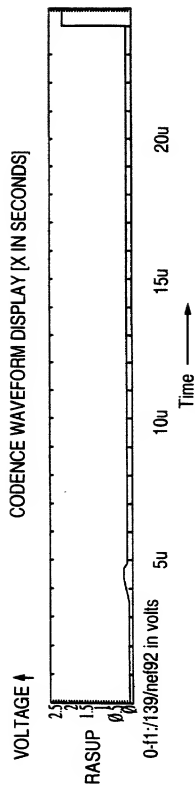
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102H**



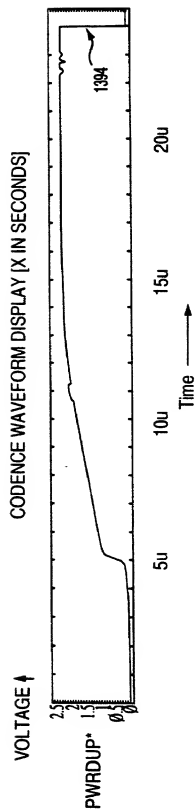
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102I**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102J**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102K**

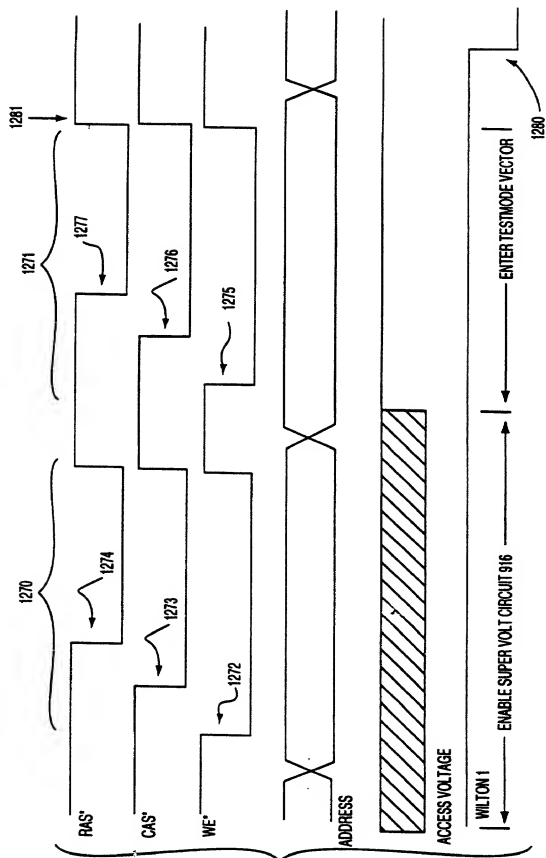


FIG.  
103



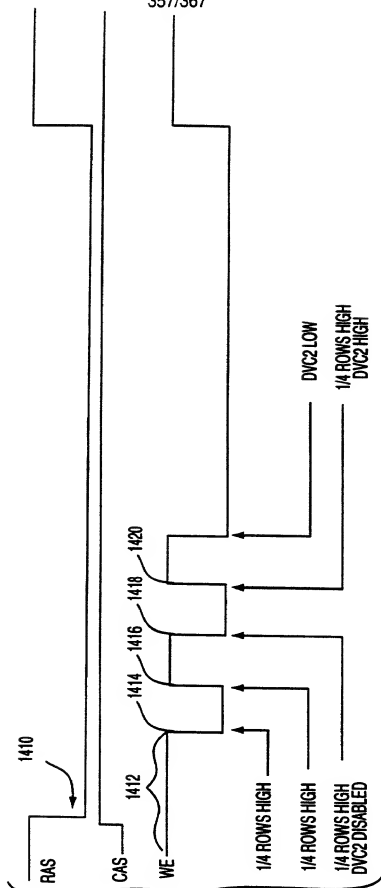
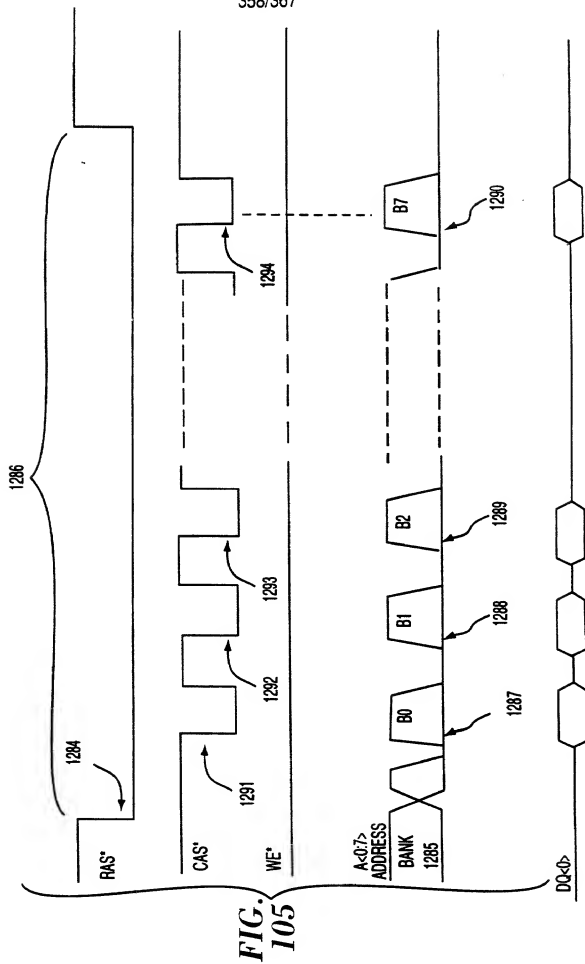
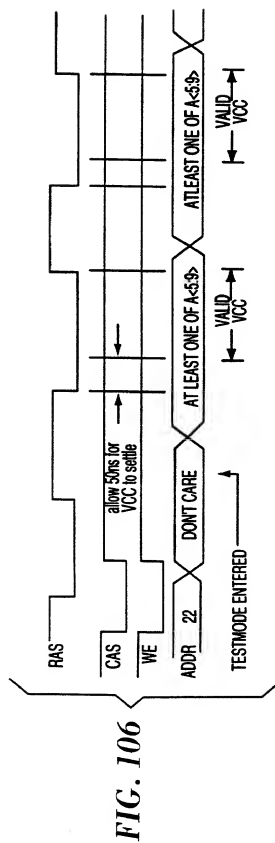


FIG. 104





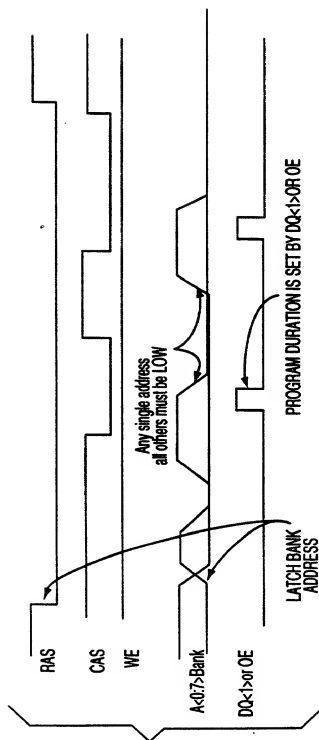


FIG. 107

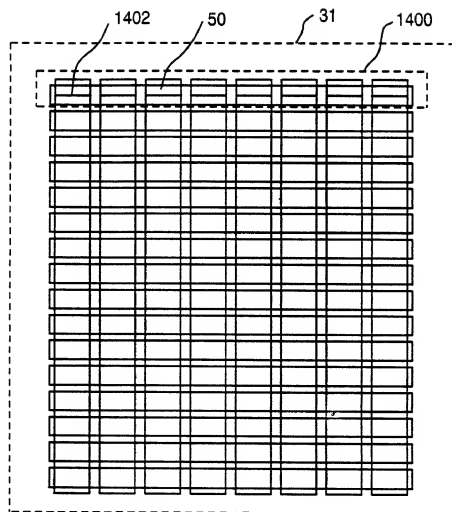
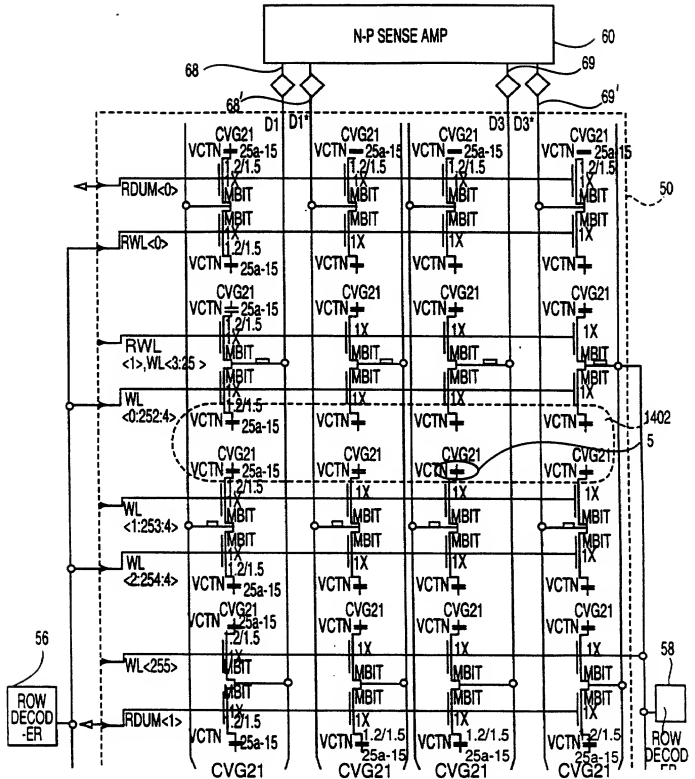
**FIG. 108**

FIG. 109-1

FIG. 109-1

FIG. 109-2



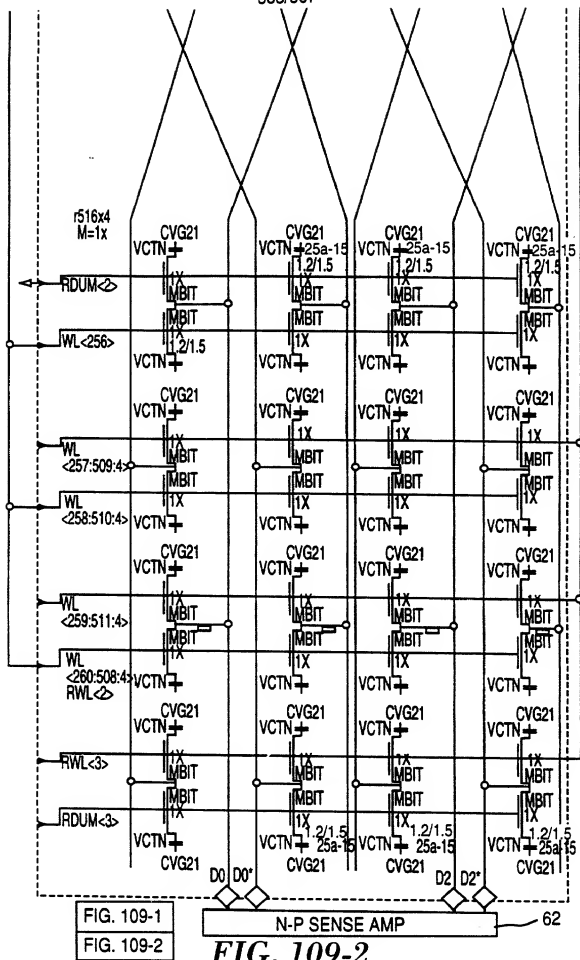


FIG. 109-2

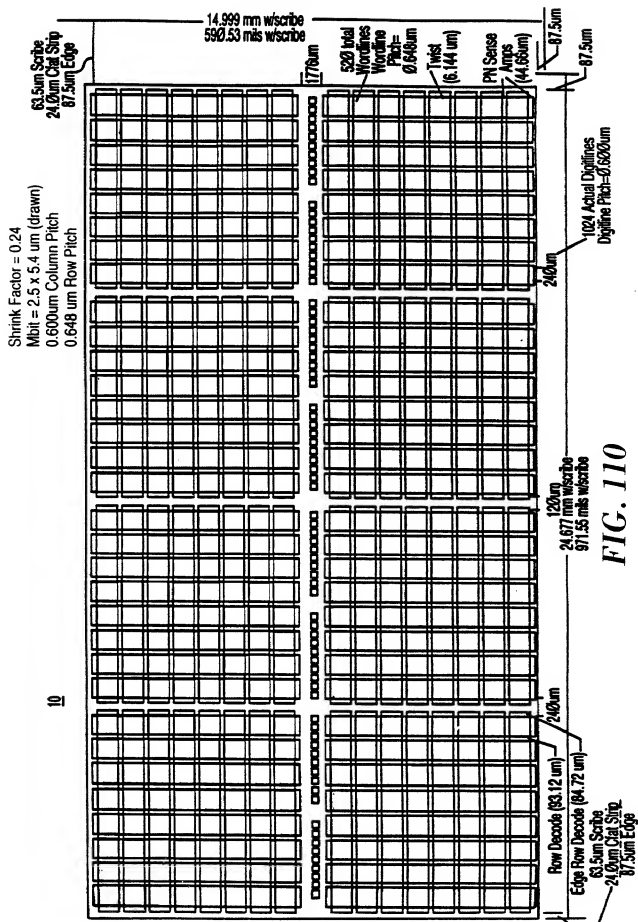
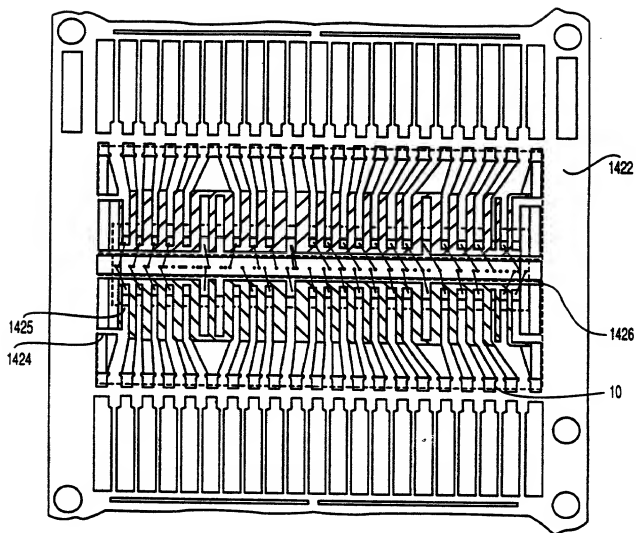


FIG. 110



**FIG. 111**



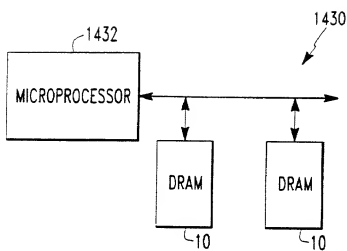


FIG. 113